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Analysis of Low Power in VLSI Circuits using Code Optimization Technique

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Abstract:

In the last few decades, integrated circuits have gone through a significant phase of development. This has given the field of IC-based technology a huge boost. However, the systems' batteries have not evolved in the same way, prompting researchers to seek for new ways based on the topic of low power design. In this work, multiple strategies for low-power digital design are compared using a variety of design metrics. Static power dissipation is a major issue in the sub-nanometer regime, where it accounts for about 80% of total power dissipation. At 0.14m, innovative stacking techniques are used to overcome static power dissipation and improve the figure of merit. Other unique techniques that are implemented on a 1-bit full adder circuit include GDI, which is utilised as a multiplexer to construct 1-bit full adders. The analysis of all in terms of design metrics, approaches are used. The uniqueness of this work is about making a design approach at 46nm that will prove to be a valuable aid in the code optimization of application-specific digital circuits which requires low power consumption.

Keywords: Integrated Circuits, Power dissipation, full adder, GDI, low power consumption

I. Introduction

The approach of constructing an integrated circuit (IC) by combining thousands of transistors into a single chip is known as VLSI. The absence of appropriate area, speed, power, application area specialization, and knowledge are, however, the general difficulties of VLSI design. Furthermore, VLSI design is challenging due to rapid technological change, the necessity for a multi-disciplinary team, the need for a large design space, and the persistence of a short design cycle.

In fact, VLSI design for achieving the best solution is cost-effective yet time-consuming. Furthermore, the design process frequently necessitates the proper selection of independent design factors. The issue of power consumption is becoming more prevalent as devices are integrated into System On Chip (SOC). To develop a more straightforward and efficient low-power coding system that can reduce consumption of power at logical levels. Various strategies have been explored to reduce the impact on logical gadgets power consumption Other power consumption approaches must also be improved[1]. As a result, rather than only power minimization, performance is a driving factor in designing and optimizing. As has been well documented, lowering power comes at the cost of some performance loss. In this trade-off, reduction in power can only win if accomplishing power minimization is more important than

circuit performance, is employed as an acceptable metric. It is not acceptable to severely reduce performance in order to accomplish power minimization. The goal of this research is to reduce power usage during data transition time.

It's never been more important to use a combination of low-power components and low-power design methodologies than it is now. As most of the components are battery-powered, miniature in size, and plenty of functionalities in the peak, the desire for lower power usage grows. VLSI designers used to prioritise space, performance, and cost while designing chips. The issue of power was the secondary issue. Because of the phenomenal expansion and advancements in the realms of personal computer devices and communication devices which are wireless, which necessitate high-speed processing and extensive functionality while using minimal power.

II. Design Methodologies with Low Power Requirements

The complicated SOCs and custom processors are critical components in embedded systems and other mobile devices, designers must carefully manage power consumption. Most consumers expect longer talk and standby times as main mobile features. Quality/Performance of these types of devices is defined by their usefulness as well as lifetime of battery. There is a market demand for smaller batteries, which in turn influences the size of the gadget and must be reduced. Reduced power dissipation of devices on a single chip necessitates device power consumption control. How much is decided on how good a design analysis is.

Device power consumption can be managed and optimised. To reduce power consumption in the final product, it's critical to estimate power early on. Understanding, designing and optimising digital circuits for various quality criteria such as power dissipation, cost, reliability, and performance are all necessary (speed). At the gate level, redundancy can occur in a circuit.

Electronic consumer component leakage power is also fast increasing, which must be addressed.

1. As system on chip technology advances, more and more functionality is integrated.

2. The introduction of mobile electronics.

3. Zero power electronics or disappearing electronics has emerged as the third and final driver for ULP design.

2.1 Sources of Power Dissipation

Three factors contribute to power dissipation in a circuit namely dynamic power, short-circuit power, and static power. Very first type is dynamic power, often known as switching power, is one of them. The majority of the electricity is wasted when charging or draining.

$$P_{dynamic} = C_L V dd^2 \alpha f \quad (1)$$

Where C_L is the load capacitance, which varies with wire length, and transistor size, and Vdd is the supply voltage, which also varies with fan-out, wire length, and transistor size. Activity has been decreasing with each consecutive process node, factor, which refers to how frequently the wires swap on average is f. The frequency of the clock is growing with each passing node for processing Leakage power, often known as static power, is a function of the switching threshold (Vt), and the supply voltage (Vdd) sizes of transistors.

Where P stands for total power. Vdd is the supply voltage, while f is the frequency of operation. The first term represents the power required to charge and discharge circuit nodes. The node capacitances are C, which is the personification of C. The second term in equation 1 of flowing current from the supply to the ground represents dissipation of power during the transitions of output[2].The static leakage power has increased exponentially as oxide thickness and threshold voltage have been reduced.

Three types of leakages generate static power dissipation in CMOS circuits:

1)leakage below the threshold

2)leakage from the gate

3)leakage from band to band tunnelling (BTBT).

Subthreshold leakage was a prominent component in all leakage in these components at technologies bigger than 130nm [5]. We may deduce from the foregoing that physical capacitance affects power dissipation, hence reducing capacitances is another way to reduce power consumption. Capacitance can be lowered by shrinking devices, however this reduces the current of the transistor, slowing its operation

2.2 Standby Power Dissipation

In VLSI circuits, there are two power dissipation modes: active and standby. The power dissipation in active mode is made up of both static and dynamic components while power dissipation in the standby condition is caused by leakage current in standby mode Furthermore, dynamic power. Dissipation also has two components: a power switch.

This occurs as a result of the charging and draining of a load short circuit power caused by rise and fall in capacitance the corresponding waveforms timings The focus of this article is on when the circuit is turned off, leakage current flows in the route between the power source and ground, causing standby power dissipation. In a standard CMOS transistor, there are generally four sources of leakage current:

1. Junction leakage current with a reverse bias

2. Drain leaking caused by a gate

3. Direct-tunneling leakage at the gate

4. Sub-threshold leakage (weak inversion)

The subthreshold leakage is the most important component that contributes the most to total leakage in CMOS devices. Sub-threshold leakage has been taken into account in this article. A minority channel is formed when the Gate to Source Voltage (VGS) of a transistor is larger than its threshold voltage (VTH).

This is referred to as a strong inversion. When a transistor's VGS is lower than its VTH, the number of minority carriers in the channel is reduced. Weak inversion is the term for this situation. A MOSFET's subthreshold current arises when the transistor's gate to source voltage (VGS) is less than its threshold voltage (VTH)[4]. When the power supply VDD is decreased below the threshold voltage (VTH) of a transistor in a CMOS design, the circuit can be run with sub-threshold current while consuming very little power. In this article, all of the circuits operate in the sub-threshold range. Scaling the supply voltage can reduce dynamic power usage by a significant amount, but this degrades the circuit's performance.

Lowering the threshold voltage value can reduce this degradation, but it comes at the tradeoff of increased leakage power. As a result, the key design consideration is lowering leakage power and completely thorough and durable strategy to reduce power dissipation in standby mode must be designed. In comparison to existing strategies, the proposed technique is more likely to achieve this goal with a substantially lower leivel of power reduction.

2.3 Circuit And Logic Style

Static CMOS and Domino are the most common basic logic styles. A static CMOS logic network is made up of two networks. A pull up network is connected to a PMOS transistor and a pull down network coupled to an NMOS transistor. The networks are built in such a way that with every given set of input, only one network is active at any given time. In CMOS, power dissipation is lower with low fan-in gates.

In a combinational gate circuit, transistor sizing can have a considerable impact on delay in circuit and dissipation of power.Although the latency of a gate lowers as the size of the transistors in the gate grows larger, the power required by the gate grows. Furthermore, owing of the increasing load capacitance, the latency of the fan-in gates rises.

Estimating or analysing a design's power consumption is the initial step in implementing power optimization strategies into a synthesis system. The downside of static CMOS is that it performs poorly in the most demanding systems. Because of the dynamic gate's improved performance.

Domino logic is extensively used in high-speed design. A dynamic logic gate differs from a static CMOS logic gate in that each gate requires less logical effort. Because of the dynamic

gate's improved performance, Domino logic is extensively used in high-speed design. A dynamic logic gate varies from a static CMOS logic gate in that each gate requires less logical effort. Because the number of transistors in the output has increased, Domino logic consumes more power.

III. Techniques Discussion

The design of the digital circuit had gone through several stages of development. Based on the results and deficiencies in terms of area, a resistive load inverter is recommended in the early stages. Depletion load nMOS followed by CMOS-based circuit topologies supplanted resistive load inverter configurations. Researchers began to think in terms of fewer devices as a result of the decision to make devices smaller and less power hungry, and CMOS was eventually superseded by dynamic CMOS and domino logic based topologies. Detailed analysis and performance are offered in the next section to provide a comprehensive knowledge of the numerous configurations that may be chosen in the near future [3].

3.1 Gate Diffusion Input

The Gate Diffusion Input (GDI) was first proposed as a new technique in low-power digital design. A simple CMOS inverter requires three inputs. The demonstration of logic CMOS circuits need to be improved, and there are a lot of them.Over the previous two decades, design techniques have evolved.GDI is a triple input approach in P is connected to the pMOS's source/drain instead of Vdd, and N is also connected to the pMOS's source/drain. connected to either the source or drain of the nMOS The P input is connected to the majority of pMOS. while the majority of the nMOS is connected to the N t.

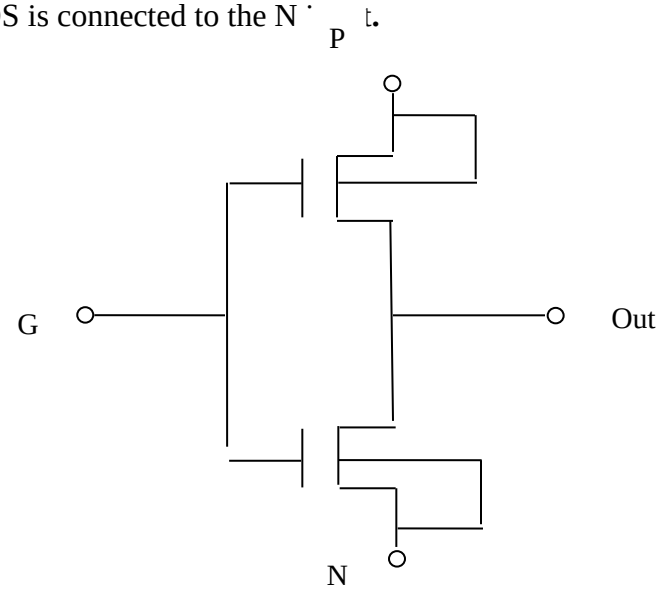

Fig 1. CMOS Inverter Using GDI

The fig 1 depicts the situation, the number of inputs for an n-input transistor is n+2. The majority of functions can be constructed with just two variables and transistors. The GDI is used as a buffer in 50% of the time utilised to restore logic levels. The GDI has its own set of drawbacks. GDI cannot be used to implement all functionalities. Although the leakage current is reduced, the GDI cell's performance diminishes below 90nm.

The area of a GDI cell is increased because separate barriers between transistors are required. In this study, a redesigned GDI cell with bulks coupled to Vdd and ground is shown. PDP is improved in this study thanks to a multi-threshold voltage approach and redesigned GDI cells, whose performance does not decline when the threshold voltage drops, thus avoiding the difficulties that plague GDI cells.

3.2 Stacking technique

Substrate currents and subthreshold leakages are the principal sources of static/leakage power. For 1m technologies, Switching Power is the most important factor. For deep submicron applications $P_{leakage}$ becomes the primary factor below 180nm. As the technology has been scaled down to the sub-nanometer level. As a result, the threshold voltage drops dramatically. Increases in subthreshold current lead to raise in leakage power. Short channel effects are amplified due to device scaling. Reduce the voltage threshold.

Technology is also scaling up. Gate oxide thickness has an impact. Because of the decrease in through the insulator, a thickness tunnelling current flows, resulting in additional power dissipation The gate oxide leakage can be caused by a variety of factors lowered by altering the dielectric constant K.

$P_{leakage}$ is a big problem since it is expected to be a major source of power dissipation in circuits that are in standby mode for the majority of the time in the coming years. To mitigate leakage power, multi threshold voltage transistors are employed in the circuit. In the MTCMOS technique, high and low threshold transistors are employed in the circuit. Low Vth transistors are utilised in speed circuits and are fast but leaky, whereas high Vth transistors are slower than other low Vth transistors but have less leakage and are used in noncritical/slow chip paths.The techniques for reducing leakage power provided in this work are classified into two categories like state saving and state destructive.

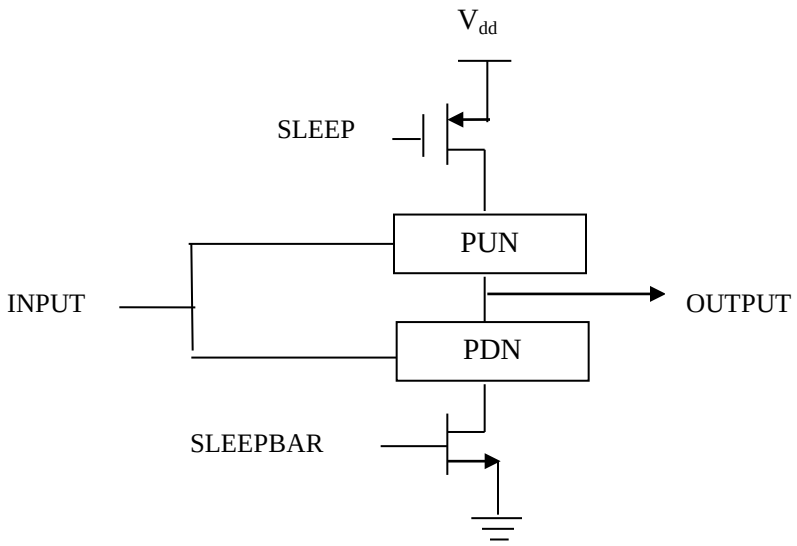

Fig 2. CMOS inverter using Sleep Technique.

3.3 Sleep technique

Sleep transistors, which are high Vth transistors connected in series with low Vth transistors, are shown in Fig 2. During the case where operation is normal in the main circuit, which consists of low Vth transistors, the sleep transistors, pMOS in PUN and nMOS in PDN, are likewise ON.

The transistors with a high threshold voltage are turned off while the circuit is in standby mode. Because high Vth transistors are coupled in series with low Vth transistors, the leakage current, which is very low, is influenced by high Vth transistors. As a result, the net static power dissipation is decreased. PUN and PDN have floating values during sleep mode and will lose status. There is a requirement for transistors to be recharged[6][7].

3.4 Sleepy Stack Technique

The "sleepy stack" is a cutting-edge leakage power reduction method that produces ultralow power in the sub-nanometer range. The sleepy stack combines the forced stack technique and sleep transistor technology. The static power dissipation in the sleep stack technique is lowered by combining FST and sleep transistors in the same circuit as one of the transistors, where the sleep transistors are either in cut off state during the sleep model or active mode during regular circuit operation[8]. The transistors given sleep as input are ON during active mode or normal mode, and they are OFF during standby mode, severing the circuit from the power rails. As a result, sub nanoscale technology achieves ultralow power. Sleep reduces power but does not maintain logic state, whereas a combination of FST and sleep does[9].

3.4.1 **Operation of circuit**

All transistors are switched on while the circuit is in normal/active mode and the sleep signal S=0 is sent to pMOS and S'=1 is given to nMOS. Since the introduction of sleep transistors, the delay has been slightly increased.During active state, are of high Vth. The drowsy stack FST is slower than switching. Sleep is aided with a high Vth. A transistor and a transistor connected in parallel to a sleep transistor reduces the amount of power that leaks out. Current is available right now transistors with a low Vth value When you're in Sleep mode, you'll be able to sleep.

Both pMOS S=1 and nMOS S'=0 are provided a signal.Even though the transistors are turned off, the logic state is maintained[10]. The force of nature the stacking of transistors reduces dissipation.

The CMOS delay can be stated as

$$T_d = KV_{dd}/(V_{dd}-V_{th})\alpha \quad (2)$$

IV. Sleepy Keeper Approach

The pMOS is connected between PUN and Vdd in this technique, and It's wired in series with the nMOS sleep transistor. Because nMOS cannot pass Vdd efficiently, the problem is solved by connecting nMOS to Vdd. Similarly, between PDN and the nMOS transistor, The output value zero is maintained in sleep mode by connecting a pMOS sleep transistor in parallel to the nMOS transistor. This approach reduces leakage power effectively[11].

The ONOFFIC approach, in which the threshold voltage remains constant, i.e. just one Vth is used, is one of the new stacking approaches performed on complete adders. Between PUN and PDN, it adds two more transistors. In both active and standby modes, the leakage power is decreased.When in the OFF state, it gives the most resistance, and when in the ON state, it provides the least[12].The pMOS drain is connected to the nMOS and the output to the PMOS, whereas the nMOS drain is connected to the circuit output and the source to PDN, and the PMOS source has connection to the power supply node VDD, pMOS is in charge of nMOS's operation.The transistors can operate in either a cutoff or a linear mode[13].

4.1 Implementation On 1bit Full Adder Circuit

Because it is one of the most basic components in digital design, the whole adder circuit was chosen. The entire adder is stacked using a variety of strategies, including sleep, forced stack, sleepy stack, multi threshold, sleepy keeper, leaky feedback approach, and ONOFIC approach[14].

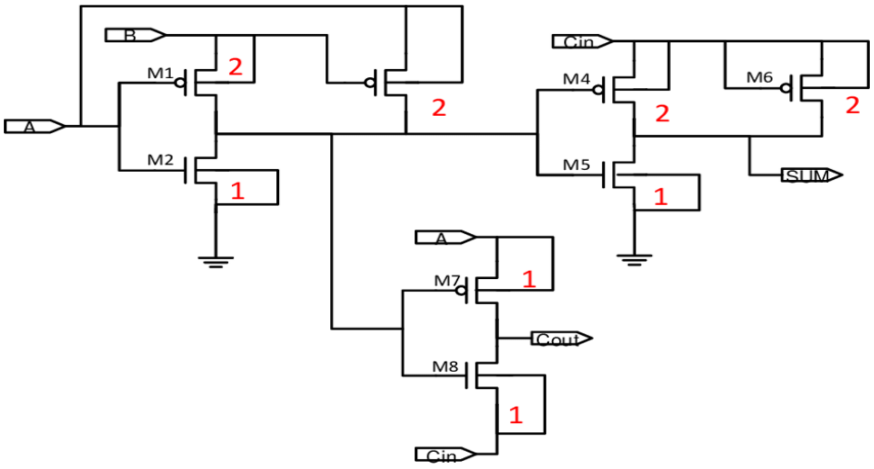

Fig 3. A 1 Bit Full Adder Circuit with modified GDI[15]

Fig 3 above depicts the Sleep transistors pMOS are connected between PUN and Vdd during sleep mode, while sleep transistors nMOS are connected between PDN and ground. The sleep transistors have a high Vth, whereas the base case transistors have a low Vth. The status of the sleep transistor cannot be saved. Each transistor is divided into two equal half-sized transistors during FST, resulting in a reduction in overall power dissipation. FST is first created using all low Vth transistors, and various parameters are measured.

V Simulation Results

On Tanner EDA Tool, simulation results for different known low power dissipation strategies and the suggested technique were achieved over various supply voltages. The 46nm CMOS technology was used to achieve minimal voltages. Schematic graph has been plotted for the data given in fig 4.

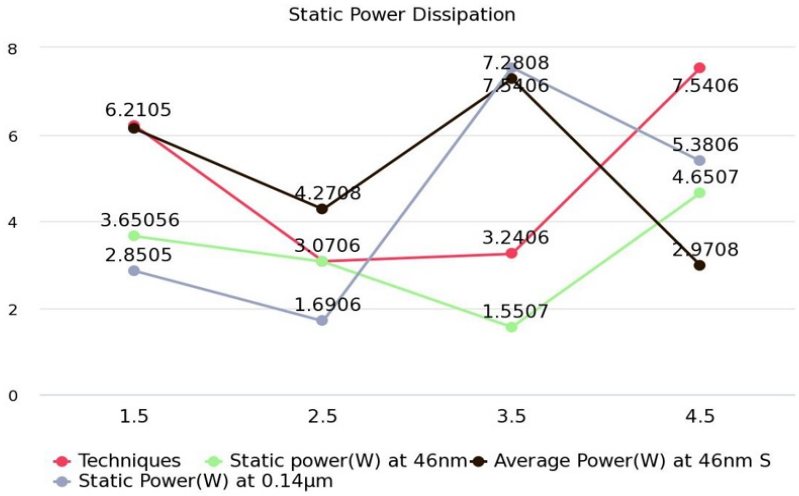

Fig 4. Static Power Dissipation at 46nm

Techniques	Static power(W) at 46nm	Average Power(W) at 46nm S	Static Power(W) at 0.14µm	Average power (W) at 0.14µm
Base Case	6.21E-05	3.65E-05 6	613E-07	2.85E-05
Sleep	3.07E-06	3.063E-07	4.27E-08	1.69E-06
FST	3.24E-06	1.548E-07	7.28E-08	7.54E-06
LFA	7.54E-06	4.653E-07	2.97E-08	5.38E-06

Table 1: Design Parameters of 1- bit full adder at 0.14µm and 46nm

Table 1 depicts the typical CMOS values of active power dissipation for Base case,Sleep, FST, LFA approaches.

Simulated Circuits Waveforms

Below from the fig 5 the waveforms for sleep approach in a 1-bit full adder at 0.14um is displayed. The frequency used is 250MHz, which means the input vector changes every 4ns. 0.01pf is the capacitance.

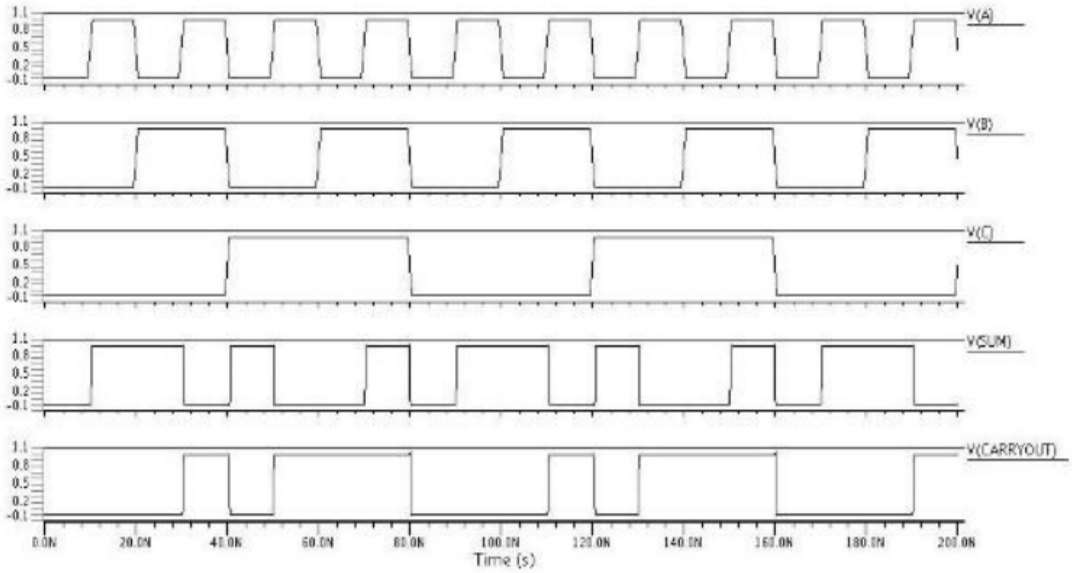

Fig 5. Waveform of full adder using GDI at 0.14µm

VI Conclusion

In comparison to the standard CMOS NAND gate, as well as previously implemented techniques such as Power Gating, Drain Gating, and Transistor Gating, the proposed technique dissipated less power. In standard CMOS implemented with a 1 bit full adder along with the modified GDI method can cut power dissipation in standby mode by 96% and helps a lot in code optimisation. Furthermore, the circuit operates in the sub-threshold range, making it ideal for applications requiring extremely less consumption of power.

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