Multiple Error Correction Using Reduced Precision Redundancy Technique

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Abstract— **The uses of FFTs are unavoidable in communication systems. As most of the information may be analog in this world and as transmission of information in digital form is more acceptable and efficient, FFTs plays an important role in present communication scenario. For a reliable communication the information that we transmit should be reached at the destination as such. But due to many factors the information that we transmits get altered. One of the main problems in communication system is soft error. Even though soft error doesn't make any physical damage to the communication system it is dangerous. It has the ability to alter the values stored in the system. It may alter the transmitted message. A lot of techniques are available to detect the soft error and correct it. Those include TMR, ECC, parity SOS, and parity-SOS-ECC. All these assume that there can only be a single error in the circuit. The proposed system known as reduced precision redundancy considers Instead of using two full precision FFTs it uses two half precision FFTs as redundant FFTs. It limits the error, reduces area and power consumption.**

Index Terms— **Reduced Precision Redundancy, Fast Fourier transforms (FFTs), Soft errors**

1.Introduction

Communication system is becoming more and more complex as the technology advances [17]. It is subjected to many errors. It is the main challenge an electronic system faces. Because of technology scaling and aggressive voltage scaling, the rate of these faults occurring in a circuit is increasing exponentially. Scaling means the transistor used are operating at low voltage and it has high tendency to affect error [10]. These faults will reveal themselves as temporary logic upsets, such as single-event upsets (SEUs) [4]. It can affect the transmitted signals and stored values which lead to incorrect or undesired outcomes in circuit and systems. A lot of researches are done academically and industrially to understand the presence of faults and the rate of increase in fault. Faults in electronic systems are divided in two types: permanent and transient. Irreversible physical defects in the circuit are known as permanent faults. The next type is soft error which is also known as transient error. It appears during the

operation of a circuit. It won't create any physical defect in the circuit. The main reasons for soft errors are cross-talk, any permanent logical error, power supply noise and neutron or alpha radiations during operational lifetime. Number of techniques can be used to protect a circuit from errors such as modifications in the manufacturing process of the circuits to reduce the number of errors by adding redundancy at the logic or system level [9]. Redundancy will ensure that errors do not affect the system functionality [5]. Other techniques includes redundancy, parity check, checksums, hamming codes, ECC, parity-SOS, parity-SOS-ECC etc. A simple ECC technique takes a block of *k* bits and produces a block of *n* bits by adding *n−k* parity check bits. XOR combinations of the *k* data bits are used as the parity check bits. It is possible to detect and correct errors by properly designing those combinations. In the case of parity-SOS and parity-SOS-ECC, SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. For the detection and correction of the errors, we can use an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. Another technique used is triple modular redundancy which adds redundancy to the circuit. Both these are algorithm based fault tolerant technique [1]. TMR has the ability to triplicates the design and adds voting logic to correct errors. It is commonly used. TMR is very effective at protecting FPGA circuits from soft errors. But it is costly in terms of the circuit area, power, and circuit timing.

FFT's protection scheme is studied and different techniques are implemented [15]. The latest technique used to reduce soft errors in FFTs is parity-SOS and parity-SOS-ECC technique. These techniques are formed by combining an existing technique known as ECC approach with the traditional SOS check. To detect and locate the errors SOS checks are used and a simple parity FFT is used for correction. Error detection can be done using an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. So in order to reduce error the expense of hardware a less expensive hardware mitigation strategy for arithmetic circuits is a technique called reduced-precision redundancy (RPR) [3]. By providing redundant, lower precision arithmetic

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circuits and comparing their results RPR can be used. It protects against large magnitude errors in arithmetic circuits. Its area savings make it an attractive alternative for protecting FPGA signal processing circuits against SEUs, transient and soft data errors. All these are single error detection and correction.

In the case of parallel FFT for multiple error detection and correction Reduced Precision Redundancy (RPR) technique can be used. RPR is a redundancy technique similar to TMR . It requires less hardware overhead by using reduced-precision (RP) arithmetic in two of its three replicas. RP arithmetic can be a good estimate of computations that use higher precision. TMR has the ability to protects the entire circuit and provides an error-free output where as RPR simply limits the error at the output of a module. The advantage of RPR over TMR is its ability to sufficiently limit the magnitude of the SEU-induced noise at a lower hardware cost. RPR has been used to protect arithmetic operations. It will reduce overheads and also reduces the area and power consumption of error correction module in a circuit. RPR is a new technique. for each circuit protected by RPR there are a number of important design decisions that must be made. Precision of RP module and determining the threshold for detecting low-magnitude errors are important. Whenever a path with delay greater than the sample period T_{samp} is excited voltage over scaling introduces input-dependent soft errors. Reduced precision module(RPR) is formed by truncating the LSB of the input bit. Soft errors appear first in the most significant bits (MSBs) since the arithmetic units employed in DSP systems are based on least significant bit (LSB) first computation. It results in errors of large magnitude. These errors degrade the performance. But these errors are desirable because they are easy to detect. In short a small fraction of input combinations excite longer paths. This fraction depends on the delay distribution of a system, which depends on the architecture. In this way the errors in the FFTs can be reduced with fewer overheads and less area and power consumption.

It is common to find several filters or FFTs operating in parallel as signal-processing circuits become more complex. This occurs mainly in filter banks or in multiple-input multiple-output (MIMO) communication systems [2]. MIMO orthogonal frequency division modulation (MIMO-OFDM) systems use parallel IFFTs/FFTs for modulation/demodulation. On long-term evolution mobile systems and on WiMax [8] MIMO-OFDM is implemented [12]. It is possible to take advantage of the parallel property of the filters or FFTS to implement ABFT techniques [6]. It can implement ABFT techniques for the entire group of

parallel modules instead of for each one independently. Initially this is studied for digital filters. Reduced Precision redundancy (RPR) can be used for parallel FFTs with fewer overheads.

In this brief, the protection of parallel FFTs is studied. The main contributions in this brief are:

(1) The proposed system for the reduction of multiple errors in parallel FFTs.
(2) Comparison with the existing technique for understanding the reduction in area.
(3) Comparison with the existing technique to understand the reduction in power consumption.

2. Existing System

This work starts with the protection scheme based on the use of parity-SOS for digital filters. In the first technique, original module consist of 4 FFTs. Input is given to each FFTs separately as x1,x, x3, x4. Here the idea is that each filter can be the equivalent of a bit in an ECC and parity check bits can be computed using addition.

Each FFT consist of a SOS check in parallel to detect the error in the FFT. The output of the Parseval check is represented as P_1, P_2, P_3, and P4. If there is any error in the FFT then the P_i will set to 1.
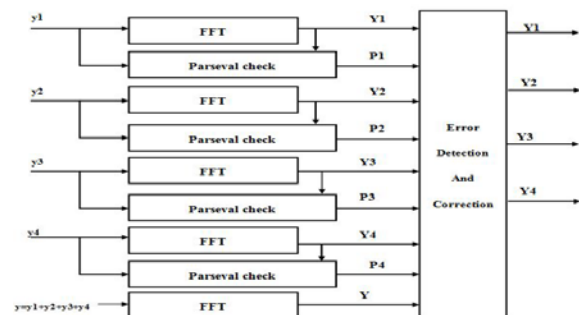

Fig 1. Parity-SOS

The output of the FFT and the P_i outputs are given to error detection and correction block. If there is any error in the FFT output then the additional FFT which is given parallel to the FFT module will correct the error. This Parseval check can only detect the errors in the FFT. It can't correct it by its own. For that an additional FFT is used. We can correct the error using its output. The SOS check can be combined with the ECC approach to reduce the protection overhead in first technique for parallel FFTs. Since the SOS check can only detect errors, the ECC part should be able to implement the correction. This is done using the equivalent of a simple parity bit for all the FFTs. The SOS check is used on each FFT to detect errors. When an error is detected then the output of the parity FFT can be used to correct the

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error. Instead of using an SOS check per FFT we can use an ECC for the SOS checks

Next technique used is parity-SOS-ECC. In this technique instead of using parallel SOS for each original module 3 SOS block is used separately which is driven by hamming code output. If there is any error in the output then the output of the Parseval check block will be set.
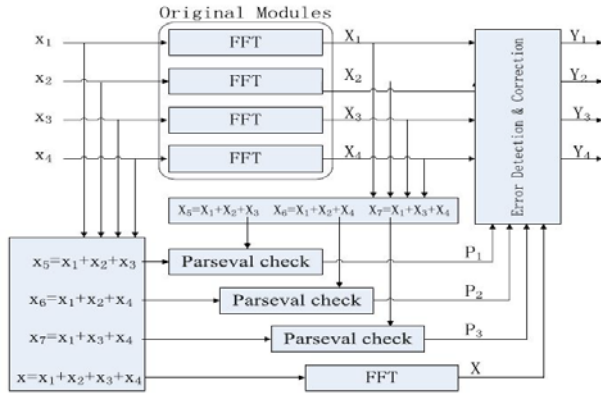

Fig 2. Parity SOS ECC

All these are single error detection and correction method. Even though these are algorithm based error correction technique it require more area for implementation as it consist of many squaring and summing blocks. So in order to reduce the area and power consumption new technique is introduced. It is an algorithmic based method.

III. PROPOSED SYSTEM

This project is detecting multiple errors and corrects it with less over heads. It's better than the traditional method known as triple modular redundancy. A less expensive hardware mitigation strategy for arithmetic circuits called reduced-precision redundancy (RPR) is the proposed project. RPR is designed to protect against large magnitude errors. It is used mainly in arithmetic circuits with the help of redundant, lower precision arithmetic circuits and comparing their results. Using of Reduced Precision Redundancy may introduce low precision errors but still its area reduction make it an attractive alternative for protecting FFTs, transient and soft data errors. There are some conditions to be satisfied while designing a RPR module. These choices include the reduced precision and threshold. RPR is implemented by creating two identical reduced-precision (RP) module of the original full precision FFTs. The outputs of the two RP modules are used to determine if there is any error in the FP module than a preset threshold, *Th*, the FP module is assumed to be in error. When the FP module is found to be in error, then it will discard the FP output and use RP output with 000's appended at the LSB part. If the FP output differs from

the RP outputs by less than Th, then it is considered as the error free output and the final output will be FP output. The arithmetic circuits protected by RPR may be of any size. The circuit used may be of basic arithmetic operation such as an adder or a more complex combination of operators and logics such as an infinite impulse response filters, finite impulse response (FIR) filter etc. This paper refers to the combination of FP module and RP module. There are two parameters to be considered before implementing RPR on a module. They are the bit width of the reduced precision module (Br) and the decision threshold (Th). The two values are linked and together greatly affect the cost and performance of RPR.
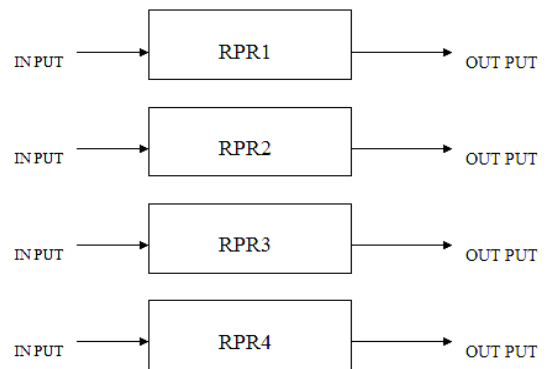

Fig 3. Block diagram of RPR technique

Fig 3 shows the diagrammatic description of this project. It is used to detect and correct errors in the parallel FFTs. Input given to this block consist of 4 inputs with each input six bit long. Each block is having the same function. Only the input will be different.
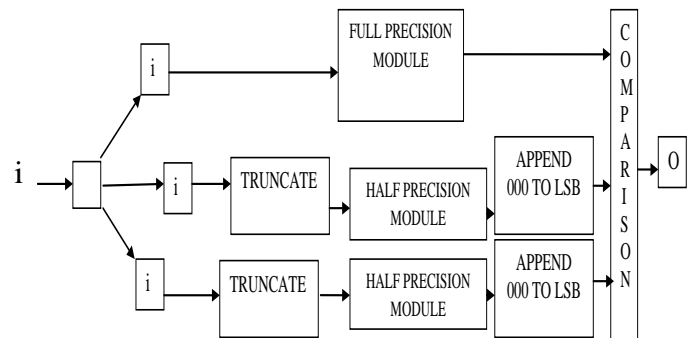

Fig 4. A single RPR module

Fig 4 shows a single RPR module. Same input is given to all these three section. First part is known as full precision module because it computes the FFT output as such i.e. the input of the FFT module is same as the input that we give at the starting section. Second and third part is known as reduced precision module because

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it uses the truncated input as the input to the FFT. Both full precision module and reduced precision module use four point FFT. Since this project is mainly intended to find out the error and correct it we are not giving much importance to FFT design. We are considering a simple radix 4 DIF FFT.

RPR module consists of three parallel paths. One consists of full precision module. Other two consist of half precision module. First input is given. Input is four points. i.e. there will be 4 inputs and each input will be six bit long. In the first part these four inputs are given as such to full precision module. Full precision module will give a four point DIF FFT output which is six bit long. In the second and third part also same six bit input is given. Then it is given to truncation block. Truncation block will truncate the six bit input to three bit input. Truncation is done by removing 3 bits from the LSB part. So the input to half precision module is 3bit inputs and output will be 3 bit output which is four point DIF FFT output. Then output of full precision module is given to the comparison block directly. But in the case of half precision module the output of the FFT is given to another block before giving to comparison. Here in this block three bits 000 is appended at the LSB part of the FFT output to make the output as six bit output. All these six bit outputs are given to comparison block. In the comparison block comparison of each output is done. There will be four outputs from each block. If the output of the full precision is less than a particular threshold value, then that output is taken as the final output. If the output of the full precision module is greater than the threshold and if the output of both the half precision modules are equal then that value is taken as the final output. Threshold value is set by doing a lot of computation. We are not comparing the outputs of all the modules directly. Instead we are comparing it with the help of a threshold value. It's mainly because truncated output is used in two half precision modules. Thus the output will be with less error. The full and half precision module we use is four point DIF FFT. Since this project is mainly for error detection and correction the FFT design is not having much importance. So we are using a simple FFT. The FFT used here is radix 4 DIF FFT.

TMR and RPR are similar in representation. But RPR has two FFTs in effect because it uses two less précised FFTs as redundant FFTs which is equivalent to one full precision module. This approach is used to limit the errors in parallel FFT. The development of the information transmission technologies in the computer networks and in the telecommunication systems is inseparably connected with the problem of integrity and of ensuring high effectiveness of error detection and correction of errors which occur during data transmission. The dynamic increase in the speed of information transmission in the buses of computer systems and the channels of computer networks brings about stringent requirements for the performance of the hardware implementation of the error detection and correction algorithm. Multiple error correction is made possible with the help of this approach.

The main issue with those soft errors mitigation techniques is that they require a large overhead in terms of circuit implementation. This overhead is excessive for many applications. for TMR, the overhead is >200%. This is because the unprotected module is replicated three times. But this approach requires fewer overheads as it is using truncated FFTs as redundant module. Another main problem of all fault tolerant system is its excessive power consumption. Many error correction systems consist of squaring and summing circuits which consumes a lot of power. This approach use less power for the detection and correction as it is not having much complex computational elements. All the existing systems only provide single error detection and correction. It is assumed that there can only be a single error on the system at any given point in time. This is a common assumption when considering the protection against radiation-induced soft errors. But this approach provides multiple error detection and correction with less area, overheads and power.

IV. EVALUATION AND RESULT

The proposed system is simulated in ModelSim SE 6.3f. A model of the communication channel is formed. In communication channels the bandwidth will be high. So the FFTs will have large inputs. This project is used for error detection and correction. So designing of FFT is not relevant, in order to evaluate the error correction capability of this technique we are taking a simple FFT. The FFT used here is 4 point radix FFT. Input is given as binary number. Six bit input is given. Initially some vales are given as input for simulation. After running the simulation if we want to check with other input we can force the required input. Before running the program clock is preset to 1. ModelSim is opened and new project is created and the program is typed in the editor. After completing the program compile the program and then start simulation. The program for running is selected and then run the program. Add waves to understand the output. First program without error is simulated. After that program with an error in FFT is simulated and its output and its waveform are observed. From the two cases it's clear that RPR method is best suited for error correction.

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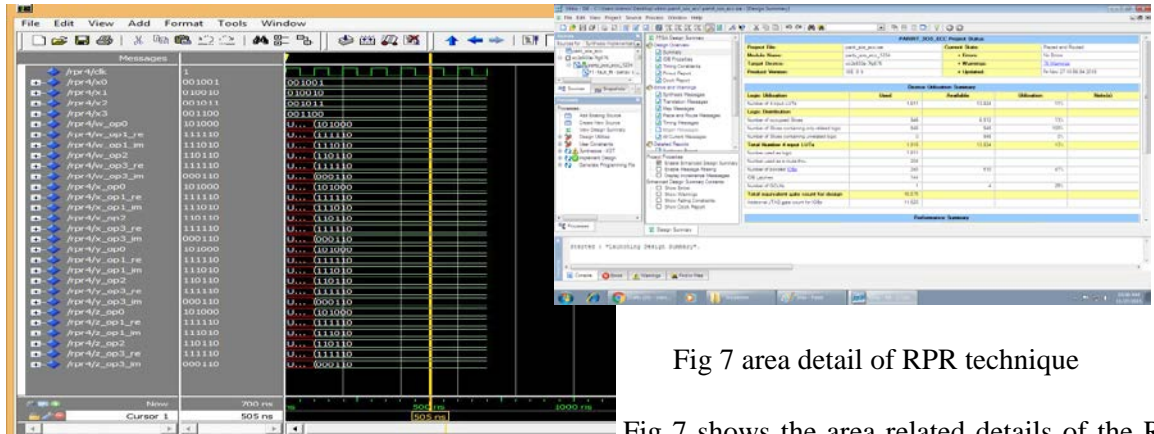*ISSN: 2395-3470*
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Fig 5. RPR output without error

Figure 5 shows the output of a four point FFT without error. The inputs given are 6 bit long. Each FFT is given 4 inputs. For easy computation all the FFT are given same input. It's possible to give different output for all these 4 FFTs. FFT used here is 4 point FFT i.e. radix 4 FFT. The input given is in the normal order. But the output is in bit reversal order. This is because the FFT use DIF algorithm. Twiddle factor $W_4^0=1$ and twiddle factor $W_4^1=-I$ is used in this FFT. The output obtained will be in bit reversal form. The output represented here is in binary format. It is possible to represent this in hexadecimal, decimal or any other form. Figure shows the input, truncated inputs and outputs of different FFTs without error.

Fig 6. RPR output with error injected

Now in order find out the efficiency of FFT fault is injected in the second bit of first output. This shows the output with error corrected. From this it's clear that using less overhead error correction technique it is possible to limit the error more efficiently.

Fig 7 area detail of RPR technique

Fig 7 shows the area related details of the RPR technique. Total number of 4 input LUTs used by the RPR techniques are 130. Number of occupied slices are 68. Total equivalent gate count for designing a RPR technique is 2124.
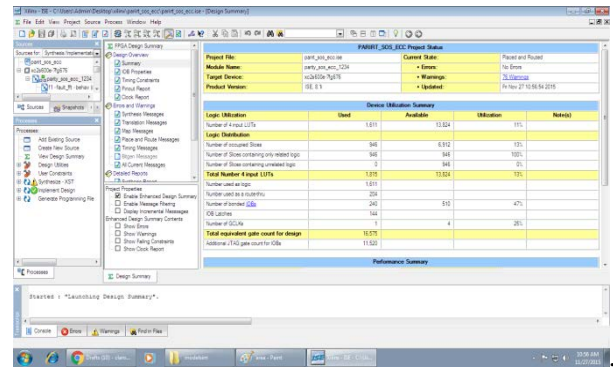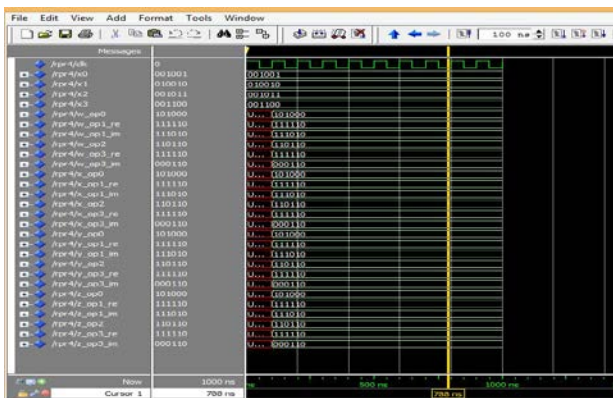

Fig 8. Area details of parity-SOS-ECC technique

Fig 8 shows the area related details of the existing technique called Parity-SOS-ECC. It uses 1611 four input LUTs. Number of occupied slices is about 946. Total number of gate count is16575.

Table 1: Performance Evaluation of Parity SOS-ECC and RPR.

	Parity-SOS-ECC	RPR
Number of occupied slices	946	68
Total number of 4 input LUTs	1815	130
Total equivalent gate count for design	16575	2124
Total power	100.66	83.77

From the above table it is clear that RPR technique uses less area for the implementation of error detection and correction block when compared to the previous technique. And the power consumption is also less.

V. CONCLUSION

Electronics system is subjected to different

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errors. In VLSI due to technology scaling and voltage scaling the faults occurring in a circuit also increased exponentially. These faults may create temporary logic upsets and can affect the signal transfers and stored values leading to incorrect or undesired outcomes in circuit and systems. A type of error called soft errors involves changes to data but wont changes the physical circuits. In many systems it is impossible to determine the correct data or even to discover that an error is present at all. This project is used to detect and correct multiple errors in FFT. The drawbacks of existing techniques are overheads, increased area and cost and single error detection and correction technique. Proposed system use Reduced Precision Redundancy (RPR) technique for the protection of FFT. In RPR along with the original module 2 less precision modules are used. The outputs of the two RP modules are used to determine if there is a fault in the full-precision (FP) module. It corrects multiple errors with fewer overheads and with less area and cost. It is clear from this output error detection and correction using RPR technique is more efficient when compared to other techniques.

REFERENCES

[1] A. L. N. Reddy and P. Banerjee, "Algorithm-based fault detection for signal processing applications," IEEE Trans. Comput., vol. 39, no. 10

[2] A. Sibille, C. Oestges, and A. Zanella, MIMO: From Theory to Implementation. San Francisco, CA, USA: Academic, 2010.

[3] B. Shim and N. R. Shanbhag, "Energy-efficient soft error-tolerant digital signal processing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 4, pp. 336–348, Apr. 2006.

[4] Byonghyo Shim, Srinivasa R. Sridhara, and Naresh R. Shanbhag, , Reliable Low-Power Digital Signal Processing via reduced Precision Redundancy

[5] E. P. Kim and N. R. Shanbhag, "Soft N-modular redundancy," IEEE Trans. Comput., vol. 61, no. 3, pp. 323–336, Mar. 2012.

[6] G. L. Stüber, J. R. Barry, S. W. McLaughlin, Y. Li, M. A. Ingram, and T. G. Pratt, "Broadband MIMO-OFDM wireless communications," Proc. IEEE, vol. 92, no. 2, pp. 271–294, Feb. 2004.

[7] J. Y. Jou and J. A. Abraham, "Fault-tolerant FFT networks," IEEE Trans. Comput., vol. 37, no. 5, pp. 548–561, May 1988.

[8] M. Ergen, Mobile Broadband—Including WiMAX and LTE. New York, NY, USA: Springer-Verlag, 2009.

[9] M.Nicolaidis, "Design for soft error mitigation," IEEE Trans. Device Mater. Rel., vol. 5, no. 3, pp. 405–418, Sep. 2005.

[10] N. Kanekawa, E. H. Ibe, T. Suga, and Y. Uematsu, Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-Magnetic Disturbances. New York, NY, USA: Springer-Verlag, 2010.

[11] S. Sesia, I. Toufik, and M. Baker, LTE—The UMTS Long Term Evo-lution: From Theory to Practice, 2nd ed. New York, NY, USA: Wiley, Jul. 2011.

[12] T. Hitana and A. K. Deb, "Bridging concurrent and non-concurrent error detection in FIR filters," in Proc. Norchip Conf., Nov. 2004

[13] Wang and N. K. Jha, "Algorithm-based fault tolerance for FFT networks," IEEE Trans. Comput., vol. 43, no. 7, pp. 849–854, Jul. 1994.

[14] Z. Gao et al., "Fault tolerant parallel filters based on error correction codes," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 2, pp. 384–387, Feb. 2015.

[15] Zhen Gao, Pedro Reviriego, Zhan Xu, Xin Su, Ming Zhao, Jing Wang, and Juan Antonio Maestro: "Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks". IEEE Transon VLSI system. June 2015.