Survey and analysis based On Highly compressed NB PHY transceiver of IEEE 802.15.6

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Abstract

IEEE 802.15.6 standard gets presented by multiple standards, like DVB, WIMAX and WLAN PHY transceiver which is multi mode, highly compressed, Hardware efficient, reconfigurable architecture of interleaver and de-interleaver Interleaver. To recover symbols from burst errors. Interleaver plays a major role in wireless protocols (3G, 4G). The perspective aim of my work is to design a modulation technique which is reconfigurable and which uses QAM, QPSK and BPSK modulations that revamp ethical self based on channel SNR. Here, we propound Bio medical signal processor using high speed and low-power memory espouse the new enact approach. Modified anti symmetric and odd coefficient accelerators are used to design LUT. The number of storage space required storing coefficients of dwt and fft will be reduced with the remould LUT. The minimization of the switching power dissipation occurs when ASOCA avoids its equivalent 2's complement values and even coefficients. Our verge on exploits state transition algorithm instead of parallel scanning codes. Subcarrier allocation algorithm peculiarly used to cornerstone on utilizing channels with high gains. Our propound model can attain a data rate of 1Gbps via to achieve 3GPP standard.

Keywords: **IEEE 802.15.6, WIMAX, BPSK (Binary Phase Shift Key), QPSK (Quadrature Phase Shift Key), QAM (Quadrature Amplitude Modulation).**

1. Introduction

IEEE metropolitan access standard (IEEE 802.15.6) is represented by WIMAX that proffers wireless broadband to fixed and firm CPEs (customer premises equipment) and mobile/cellular terminals. The network renders a wide variety of services counts multimedia, voice and data established on the IEEE 802.16-2004 standards, bandwidth in a wide Frequency range can be efficiently allowed for usage in WIMAX, and broadband internet access it can be Used as a last mile solution. In cursory an address generator for reconfigurable Interleaver/De-interleaver is used for increasing speed of the WIMAX transceiver. The literature survey of the breathe papers are described about undeniable merits and demerits is used to make new approach of implementation. WIMAX physical layer model is increase the performance evaluation. But this model build using MAC PDU by physical layer .Using LUT based address generator for Interleaver/De-interleaver is combining the incoming data streams into a block can reduce the continuous memory access . 1/2 code rate based address generator is used for FPGA implementation of the Interleaver of WIMAX (IEEE802.15.6 standard) .FSM based same interleaver is used for increasing the speed of the WIMAX system. It uses permissible code rates and modulation schemes.2D realization of the interleaver is used to reduce the memory to achieve hardware efficiency.

LUT's root technique has the lengthy expression and complicated. Compare to [base paper number] LUT technique is slow in operation and consuming large logic resources.Mathematical algorithm is developed to eliminate the requirement of floor function. It makes the low complexity for FPGA implementation. Mathematical algorithm makes low-complexity architecture for address generator when digital hardware is realize. The block interleaver is make complexity when block size is large. Fixed modulation is used in QPSK, BPSK and QAM. Because of Fixed modulation Speed of the WIMAX transceiver will reduce. Interleaver/De-interleaver is not reconfigurable, so process of interleaving/de-interleaving process will take more time. For that proposed hardware architecture is introduced. This architecture is modeled in Verilog and implemented in Altera.

2. Previous Work

In the year 2007 (Jan) the paper titled a low power 2.45 GHz zigbee transceiver for wearable personal devices in WPAN authored by C.C. Wang, J.M. Huang, L.H. Lee, S.H. Wang and C.P. Li and the paper is description is that It is used which is compatible with the physical layer of IEEE 802.15.4 standard for independent channel transmission .and the drawback is that it is Incompatible for 4G networks. In the year 2013 the paper titled An Ultra Low-Power and Area-Efficient Baseband Processor for WBAN Transmitter authored by Mengyuan Chen, Jun Han, Dabin Fang, Yao Zou and Xiaoyang Zeng and the paper description is that DPSK Modulator is optimized by employing canonical signed digit coded filters for low power and area-efficiency consideration. and the drawback is that Higher power consumption due to large number of pipeline latches at PP generation.In the year Nov. 2014 the paper titled Hardware implementation of NB PHY baseband transceiver for IEEE 802.15.6 WBAN authored by Mathew.p,Intern, CDAC, Bangalore, India Augustine,   L. Kushwaha,   D. Vivian, D. Selvakumar,   and the paper description is that Wireless body sensor network with low power consumption during Transceiver is presented for short range communications. Also Higher frequency is used for communication with smaller antenna for information transmission. And the drawback is that predetermined transmission range & signal interpolation due to short range communication License free communication frequency could be only used. In the year 2010 the paper titled Wireless Patient Monitoring System authored by Radosveta Sokullu, Mustafa Alper Akkau, Huseyin Erturk Ceti and the paper description is that Wireless patient monitoring system was proposed as a prototype to minimize the power consumption and the costing problems. Visual Basic Net. 2010 as the software and Peripheral Interface Controller (PIC) 16F877 microcontroller as the paraphernalia circuit were used with full duplex communication. And the drawback is that PIC based system design would perform with lower data rate with. Also requires manual operation for custom software evaluation. In the year 2010 (sep) the paper titled Narrowband Physical Layer design for WBAN system authored by BoKeun Choi , ByungSoo Kim, SangSeol Lee and

The paper's essence is that the design of PHY simulator for WBAN system in IEEE 802.15.6 is proposed with the modulations method is changed by frequency band and data rate for variable communication range. And the drawback is that for long range communication, higher beam foaming is required to adapt variable frequency transmission for fast fading channels. In the year 2013 (nov) the paper titled The design and implementation of IEEE 802.15.6 Baseband on FPGA authored by Yunping Liang, Yu Zhou, and Ye Li and the paper description is that Real time implementation is presented to show efficiency of IEEE 802.15.6 in Xilinx FPGA's with throughput of 187.5kbps. and the drawback is that For multi mode transmission, this system achieved lower data rate compared to 4G standards (WIMAX, LTE).In the year 2014 (July) the paper titled Hardware Implementation of (63, 51) BCH Encoder and Decoder for WBAN using LFSR and BMA authored by Priya Mathew, Lismi Augustine, Sabarinath G., Tomson Devis and the paper description is that for forward error correction BCH Encoder and Decoder is implemented .It can detect and correct up to 2 random errors. and the drawback is that BCH has Low error correction and High transmission overhead .In the year 2006(sep) the paper titled A WBAN-based System for Health Monitoring at Home authored by Otto, C.A. Lewis avant-garde Technol. Inc., Huntsville, AL Jovanov, E. Milenkovic and the paper description is that A prototype system for continual health monitoring at home and the drawback is that Slow data transmission. In the year 2012(may) the paper titled A distributed wireless body area network for medical supervision authored by Changhong Wang stream of Control Science and technology Harbin Institute of Technology, Harbin, China Qiang Wang , Shenzhen Shi and the paper description is that The system contains three layers: sensor network tier, mobile/cellular computing network tier, and remote monitoring network tier. It provides congregate, demonstration, and storage of the vital information such as electro cardio graph, oxygen in blood, temperature of the body, and rate of respiration. And the drawback is that large area. High power consumption.

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2. The Repose of the Paper

2.1 System description

Figure 1 displays block diagram of a simple WIMAX System. The transmitter block used Signal generator, Serial to Parallel converter, Convolution code encoder, convolution interleaver, adaptive modulator, pilot carrier insertion, inverse FFT (IFFT), and guard interval insertion. The orthogonal frequency division multiplexing (OFDM) is one of the modules in the WIMAX system which supports many modulation schemes to implemented by performing FFT and Inverse FFT on the input data stream First data is coming from the signal generator and it will convert serial to parallel using STP converter. Converted input data stream is encoded by Forward error correction coding technique namely convolution code (CC) encoder. Reduces the burst error using Convolution interleaver. Pivoting on the channel conditions the wireless system chooses the highest order of modulation with the use of adaptive modulation. As we could expand the range, we can step down to lower modulations (in other words, BPSK), but we are closer to utilize higher order modulations like QAM for throughput to be increased. In incorporation, fading and other interference are tamed by the system using adaptive modulation. The restoration of the original data sequence at the output is enabled when the blocks are systematized in reverse order in the receiver.
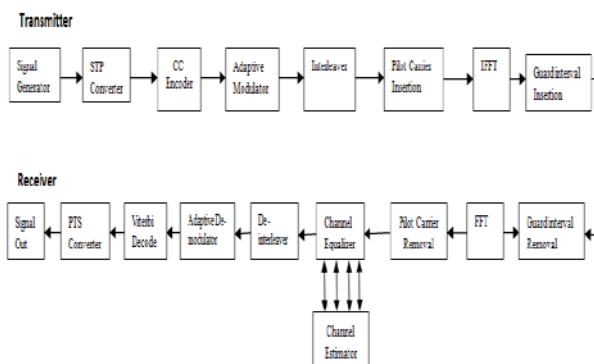

Fig.1. Structure of WIMAX Transceiver

2.2 Adaptive Modulation

The signal enters the modulation block once it has been coded. To map coded bits to a formation that can be effectively mediated over the communication channel all the wireless communication systems use a modulation scheme. Here thus, the bits are mapped to a phase and subcarrier amplitude, which is depicted by a Quadrature-phase (IQ) vector and complex in-phase .Adaptive Modulation and Coding.

The particularized modulation scheme in the uplink (UL) and downlink (DL) are quaternary PSK, binary phase Shift keying, 64 (QAM), 16 (QAM) and. To form burst profiles, The FEC options are paired with the modulation schemes. To attune bits to the complex constellation points. Seven combinations of modulation and coding rate are particularized by the PHY, which can be assigned exacting each subscriber, in UL and DL. There are commutates in Between data rate and robustness, pivoting on the propagation conditions. Table 1 shows the combination of those modulation and coding rate.

Modulation	Uncoded Block Size (bytes)	Coded Block Size (bytes)	Overall Coding rate	RS code rate	CC code rate
BPSK	12	24	½	(12,12,0)	1/2
QPSK	24	48	½	(32,24,4)	2/3
QPSK	36	48	¾	(40,36,2)	5/6
16-QAM	48	96	½	(64,48,8)	2/3
16-QAM	72	96	¾	(80,72,4)	5/6
64-QAM	96	144	2/3	(108,96,6)	3/4
64-QAM	108	144	¾	(120,108,6)	5/6

Table 1. Channel coding

If low SNR, in order to improve fidelity the signal constellation size is reduced. To make transmission more robust lowering the effective SNR is done. Confabulate, in periods of low fade or high gain (high SNR), to allow higher data rate attune schemes to be employed with low probability of error the signal constellation size is increased .Thus ameliorate the expeditious SNR.

2.3 Interleaver/Deinterleaver Structure

The block permutes the symbols in the input signal IS convolution interleaver. A set of registers is used initially. The register length step parameter the delay value of the kth shift register is (k-1) times. The value of the row of shift registers parameter is it registers the number of shift. The block of the Interleaver/Deinterleaver in the WIMAX system

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shown in figure 2. It has the two memory blocks, namely M-1 and M-2 with read/write address generator. In the interleaving block one memory block is onset to write means another memory block is onset to read and this process will continue vice versa. When sel = 1, write is enabled M-1 is active. During this time period input data stream is written in M-1 means and receives the write address. Concomitantly, input data stream is read from M-2 memory with supplied of read address. After finish the read/write process in memory block up to their covet memory location as particularized by interleaver depth, the status of the sel signal is changed the operations. The block interleaver/Deinterleaver operates with different depths to various code rates and modulation schemes (table 1) for IEEE 802.15.6. Here, the block size corresponding to the number of coded bits per allocated sub-channels per OFDM, d represents number of columns of the block interleaver which is quintessentially chosen to be 16 for WIMAX. The outcome after initial level of the permutation and the **k** changes from 0 to N_{cbps} -1. **s** is a parameter defined as **s**= $N_{cbpc}/2$, where **N_{cbpc}** is the number of coded bits per sub-carrier, and that is exactly, 2, 4 or 6 for QPSK, 16-QAM or 64-QAM respectively.

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth,Ncbps in bits	96	144	192	288	288	384	432
	192	288	384	576	576	–	–
	288	432	576	–	–	–	–
	384	576	–	–	–	–	–
	480	–	–	–	–	–	–
	576	–	–	–	–	–	–

Table 2.In IEEE 802.15.6 for All Code Rates and Modulation Schemes of Permitted Interleaver and Deinterleaver Depth.
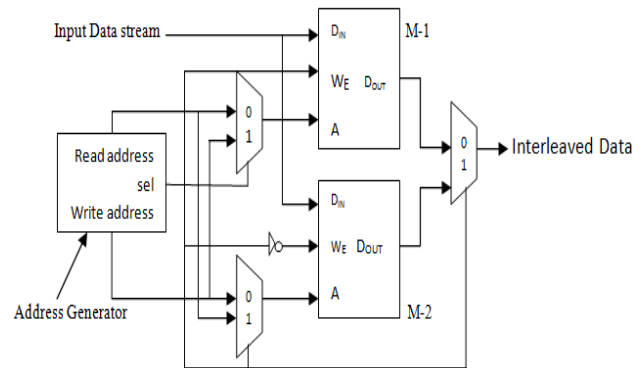

Fig 2. Block diagram of Interleaver/Deinterleaver structure.

2.4 Proposed Algorithm

For multiple user orthogonal frequency-divisions multiplexing networks an adaptive modulation scheme is presented. The eventual point of disembarkation goal of the scheme is to diminish the total transmit power with a constraint on the transmission rate for the users, presuming mastery of the prompt channel gains for all users using a bonded bit-loading and subcarrier allocation algorithm. The propounded subcarrier assigned algorithm particularly directs on using channels with high gains. Thus, in the manifestation of two or more users with higher channel gains than threshold αth, selected by trial and fallacy in a certain subcarrier, the choice of that subcarrier is relinquish to the subcarriers that are allocated when the rest of the subcarriers are assigned to the users with the highest gain.

2.5 Simulation Result

The proposed hardware of the address generator of reconfigurable Interleaver/Deinterleaver is converted into a Verilog program using Altera. The simulation result is shown in figures below. In initial process shows the multiple address generation for the Interleaver/Deinterleaver. The adaptive modulation and demodulation is produced the simulation output using all permissible modulation type and code rate adaptively. That the Simulation result is produced using Modelsim-Altera 6.6c (Quartus II).

3. Table

COMPARISON TABLE:

PARAMETERS	EXISTING OUTPUT	PROPOSED OUTPUT
TOTAL LOGICAL ELEMENTS (AREA)	158/8.256(2%)	108/8.256(1%)
TIMING ANALYSIS	118.11MHz	104.3MHz
DYNAMIC POWER DISSIPATION	8.49 mW	4.83 mW
STATIC POWER DISSIPATION	25.68 mW	25.64 mW
I/O POWER DISSIPATION	51.01 mW	31.76 mW
TOTAL POWER DISSIPATION	85.18 mW	62.23 mW

Table 3.In IEEE 802.15.6 based comparison output

4. Conclusions

In this paper design of WIMAX transceiver described by Verilog is simulated using Modelsim 9.1 and targeted on Altera cyclone .The proposed address generator for wimax reconfigurable interleaver, de-interleaver supporting all attainable code rates and modulation patterns as per IEEE802.15.6 is obtained and compared and better results are obtained for future research .

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