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Enhanced Low Power Pulsed Triggered Flip-Flop Design Based on Signal Feed Through Scheme With Voltage Scaling

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Abstract

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. In this project a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic is done. The key idea is to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The power dissipation of all the P-FF with voltage scaling are simulated and lowest one is proposed.

Keywords: *Flipflop, Pulse Triggered Flip Flop, Low Power.*

1. Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique.

In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data “1” and “0,” the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal.

2. Pulse Triggered Flipflop

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type
P-FFs are in general more power-economical. However, they suffer from a longer discharging path,

which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

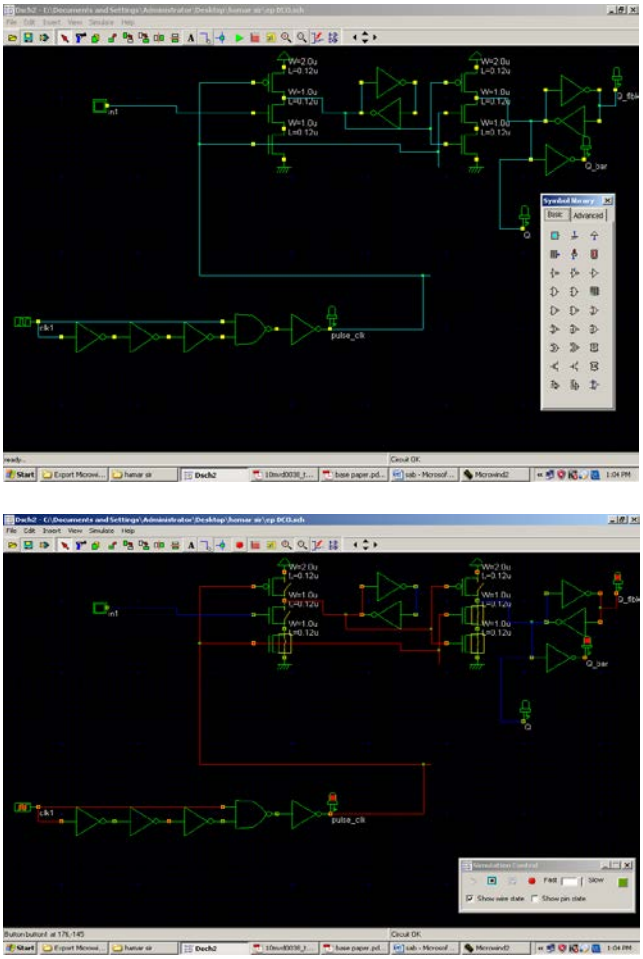
To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-close to-output (ep-DCO). It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed. Fig. 2(a) shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1."

In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only. Fig. 3(a) shows a similar P-FF design (SCDFF) using a static conditional discharge technique. It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flipflop (MHLFF) shown in Fig. 4(a) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.

3. Implementation

1. ep-DCO:



Fig(a).Implementation of ep-DCO.

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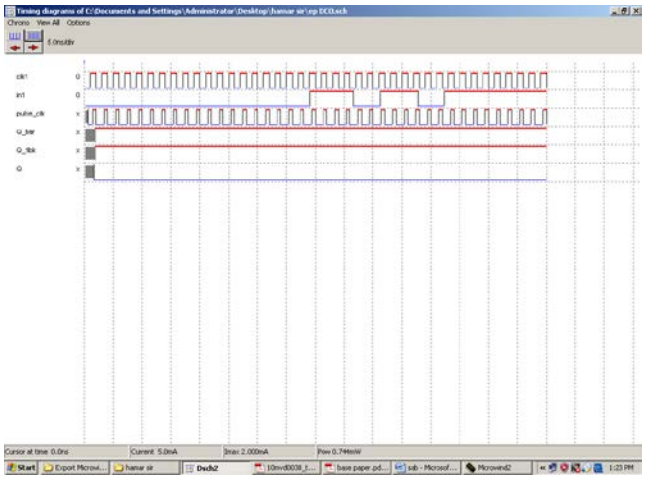
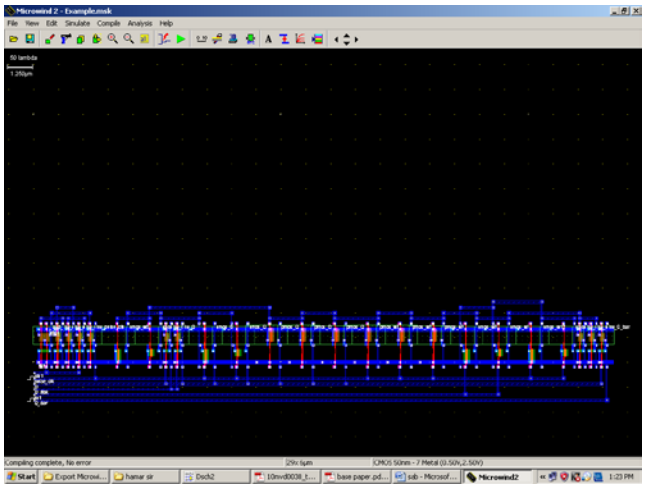


Fig (b).Timing diagram



Fig(c).Layout

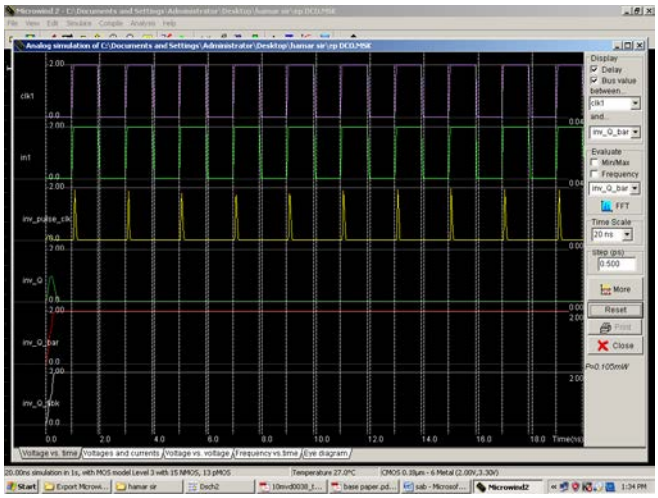
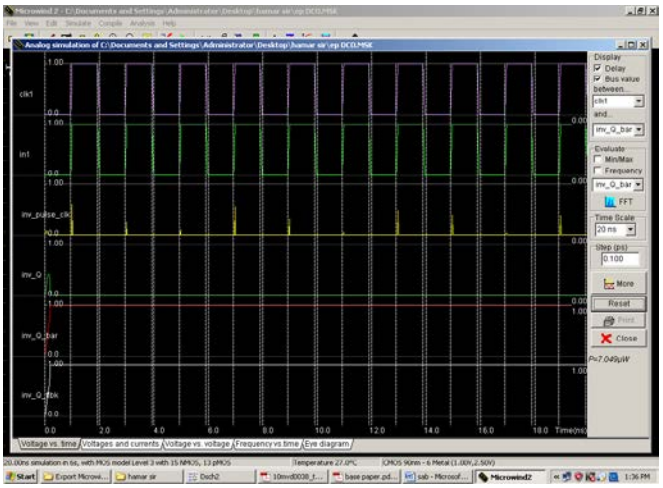


Fig (d).Simulation of180nm technology.



Fig(e).Simulation of 90 nm technology

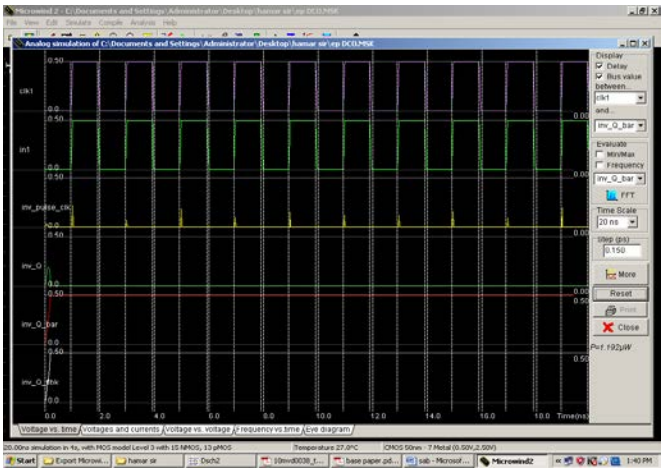
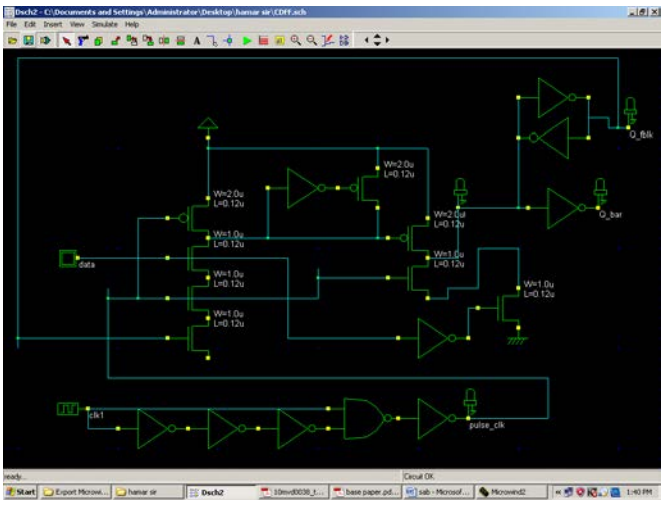


Fig (f). Simulation of 50 nm technology

2. CDFF:



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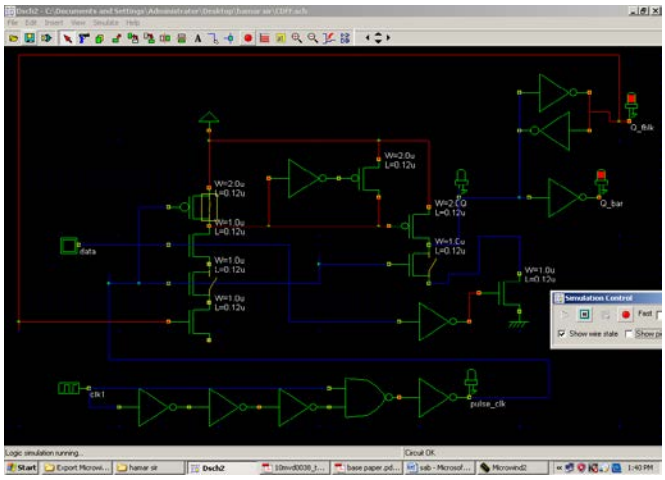
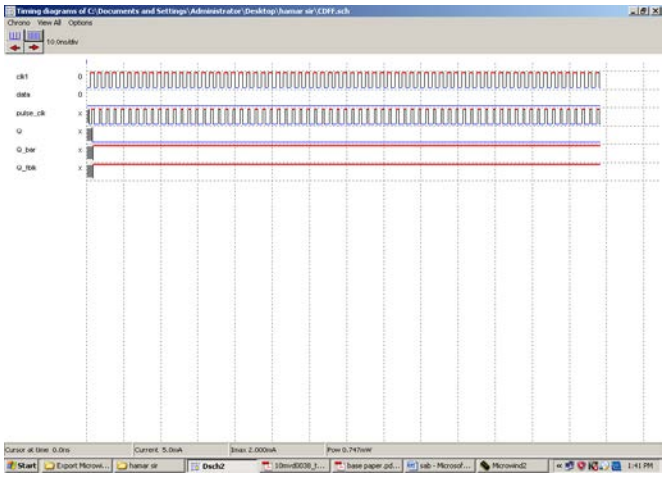
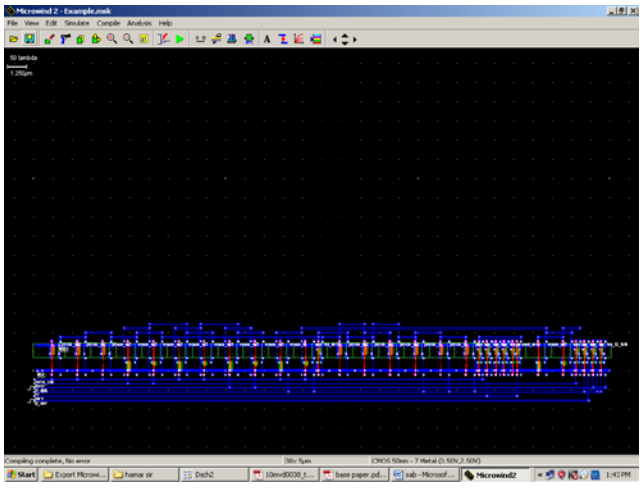


Fig (a). Implementation of CDFF



Fig(b).Timing Diagram



Fig(c).Layout

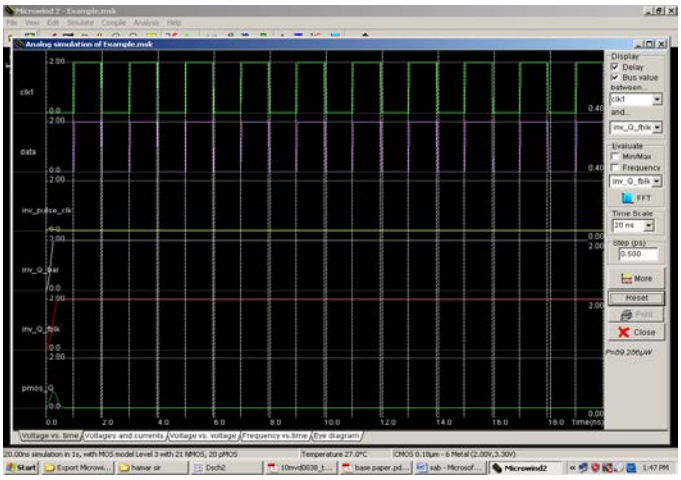
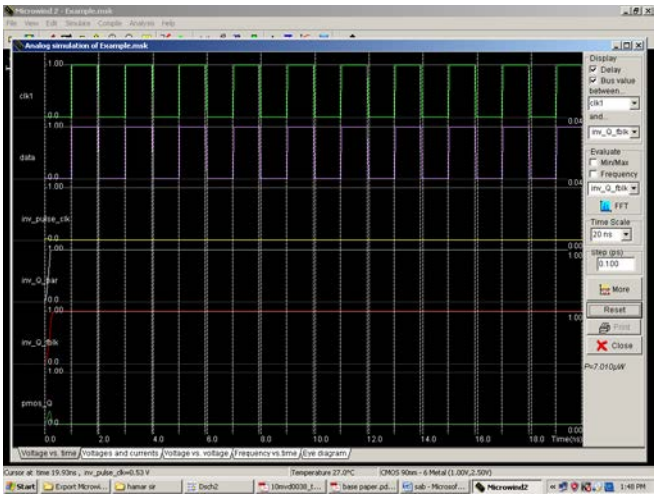


Fig (d). Simulation of180nm technology



Fig(e).Simulation of 90nm technology

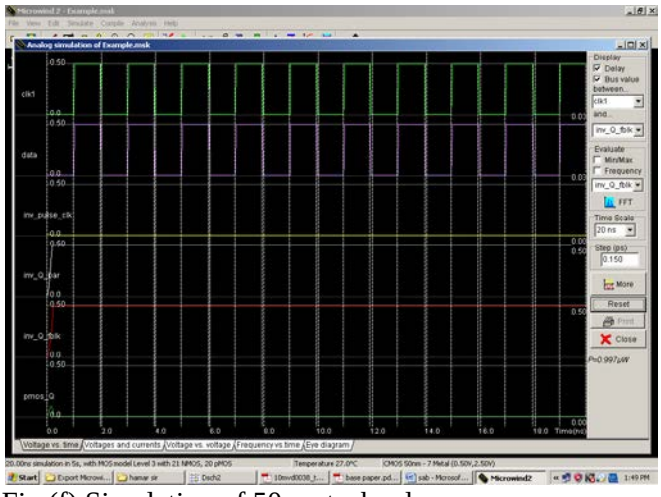


Fig (f).Simulation of 50nm technology

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3. Static CDFF:

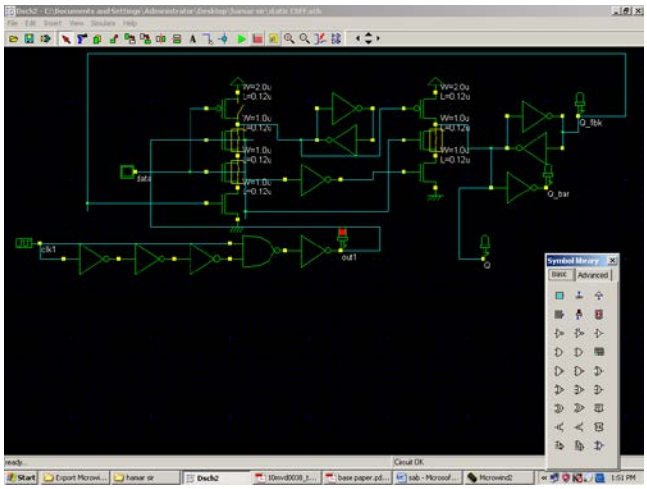

Fig (a). Implementation of SCDFF

Fig (b). Timing diagram

Fig (c). Simulation of 180nm technology

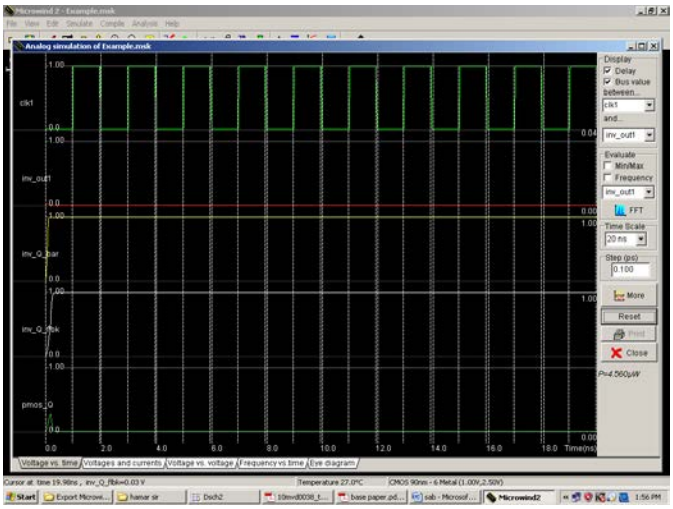

Fig (d). Simulation of 90nm technology

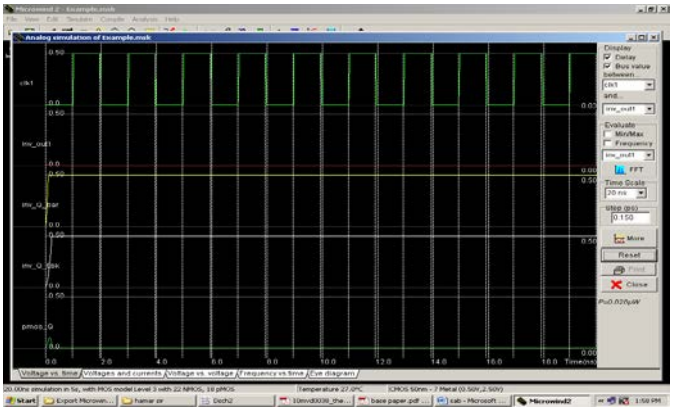

Fig (e). Simulation of 50nm technology

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4. MHLFF:

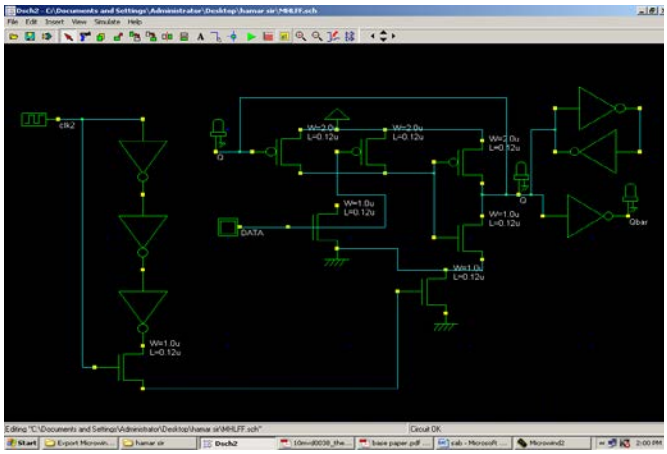

Fig (a). Implementation of MHLFF

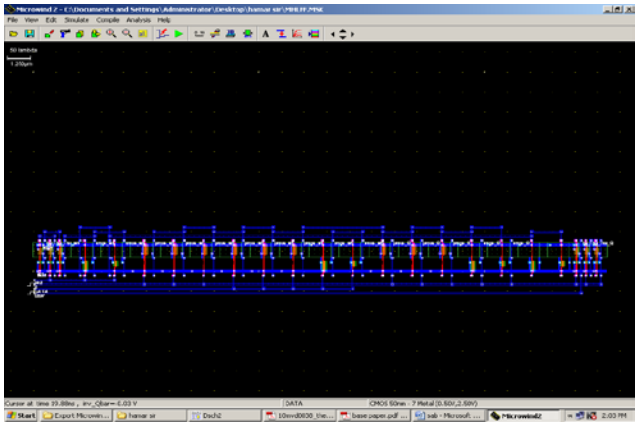

Fig (b). Layout

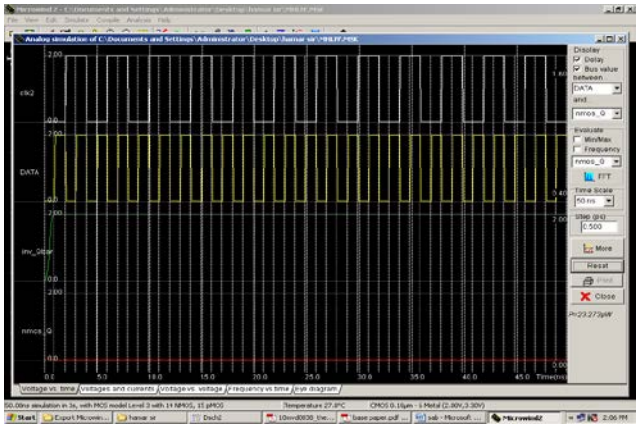

Fig (c). Simulation of 180nm technology

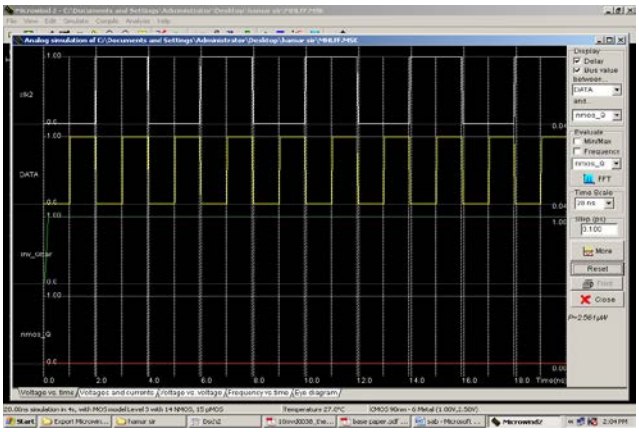

Fig (d). Simulation of 90nm technology

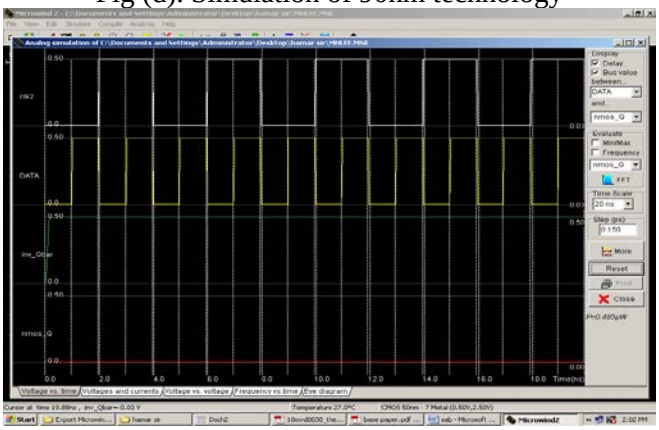

Fig (e). Simulation of 50nm technology

Table 1: Power dissipation of pulse triggered FF

POWER DISSIPATION						
SLNO	***TECHNOLOGY nm***	***PG BLOCK***	***ep DCO***	***CD FF***	***STATIC CD FF***	***MHFF***
1	180	42.843µW	0.105 µW	9.286 µW	62.895 µW	23.273 µW
2	120	7.202 µW	4.526 µW	13.091 µW	9.233 µW	18.824 µW
3	90	3.276 µW	7.049 µW	7.610 µW	4.560 µW	2.561 µW
4	65	2.355 µW	6.05 µW	4.699 µW	3.266 µW	1.657 µW
5	50	0.45 µW	1.192 µW	0.997 µW	0.828 µW	0.485 µW

4. Applications of flip-flops:

Event Detect, Data Synchronizer, Frequency Divider, Shift Register**,** counters, Parallel Data Storage, Data Transfers etc.

5. Power Dissipation in flip-flops:

The power dissipation in flipflop majorly observed in different aspects they are

- Power and Energy
- Dynamic Power
- Static Power
- Low Power Design

In those, we are proposed mainly on Dynamic power dissipation.

- Dynamic power is required to charge and discharge load capacitances when transistors switch.
- Suppose the system clock frequency = f, Let f_{sw} = af, where a = activity factor, If the signal is a clock, a = 1, If the signal switches once per cycle, a = ½,
- Dynamic gates:
  Switch either 0 or 2 times per cycle, a = ½

Dynamic Power:

$$P_{dynamic} = \alpha C V_{DD}^2 \mathrm{f}$$

6. Conclusions:

Here we have designed enhanced low power pulse triggered flipflop based on signal feed through scheme with voltage scaling in different technologies. Low power consumption is seen in 50nm technology.

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