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Inverting step-up converter

Felix A. Himmelstoss, Gabriel Hochmeister, Dominik Petrovic
Faculty of Electronic Engineering and Entrepreneurship,
University of Applied Sciences Technikum Wien, AUSTRIA

Abstract

Starting from a negative output super-lift converter which has high repetitive input current peaks an improved version is derived which avoids these peaks. The function of both converters is treated and the design explained. Compared to typical step-up converters the converter has no inrush current, when applied to a stable input voltage source. The voltage stress of the electronic switch and the diode is the same as for a noninverting Boost converter. Although the converter needs two capacitors and two coils, the dynamics of the system can be described by a second order system which simplifies the controller design. The large and the small signal models are derived. A feed-forward control is shown. Simulations and some measurements are also included.

Keywords: *DC/DC converter, inverting Boost, dimensioning, modelling, transfer function, feedforward control.*

1. Introduction

There are several possibilities to produce a negative voltage out of a positive one. For small power (a few Watt) simple switched capacitor converters can be used. For higher power it is much more efficient to use energy conversion by a magnetic field. Classical power converters to produce a negative voltage are the Cuk and the inverting Boost converters. These and other possible topologies are treated in the textbooks e.g. [1-3]. A comprehensive review on step-up converters is given in [4]. Over hundred DC/DC converters are shown in [5]. The starting point for this investigation is the negative output super-lift converter [6]. This is an interesting inverting step-up converter, but has the disadvantage of a high peak current. In this paper some improvements of this converter are presented and explained.

2. Fundamental analysis

For the basic explanation ideal components are supposed, that means no parasitic resistances and extremely fast switching. The electronic switch is drawn as a MOSFET. Of course other switching devices can be used. For the explanation we follow [7].

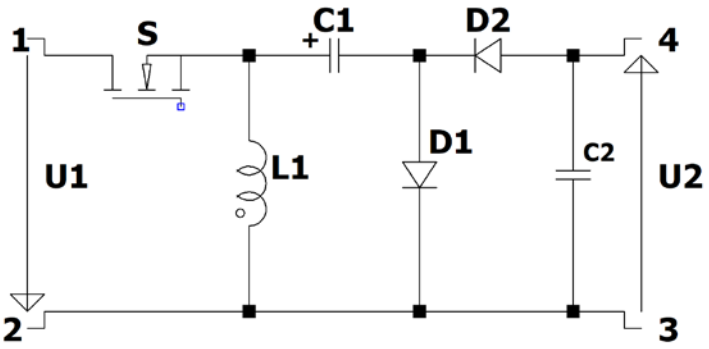

Fig. 1 Negative output super-lift converter.

The starting point, a negative output super-lift converter is drawn in Fig. 1. The converter consists of an electronic switch S, two diodes (D1, D2), two capacitors (C1, C2), and a coil L1. The input voltage is connected to the input terminals (1 is the positive and 2 is the negative input connector), the load is connected to the

output terminals (3 is the positive, 4 is the negative output connector). Two modes can be distinguished. During mode M1 the active switch S is turned on, and in mode M2 the active switch is off and the diode D2 is conducting. During M2 the current through L1 has commutated into D2, which is in series with the parallel connection of the output capacitor C2 and the load and in this way supplies the output. The voltage across C1 decreases. When S1 is turned on again, the current through L1 commutates into the switch S and the diode D2 turns off. Now also a second loop occurs: the voltage across C1 was reduced during M2 and is now lower than the input voltage U1, therefore D1 turns on and C1 is charged up to U1 by an additional current peak. In the stationary case one can set the voltage across C1 to U1 (the capacitor C1 is so large that the voltage across it is nearly constant during one switching period). One can write therefore

$$U_{C1} = U_1 . \tag{1}$$

The voltage-time balance of the inductor L1 (in the steady-state the voltage across an inductor is zero in the mean) can therefore be written as

$$U_1 d = \left|U_{C1} - U_2\right|(1-d) = (U_2 - U_1)(1-d) . \tag{2}$$

Now one can easily determine the voltage transformation ratio M of the converter according to

$$M = \frac{U_2}{U_1} = \frac{1}{1-d} \ . \tag{3}$$

The voltage transformation ratio is the same as that of the classical step-up converter. The directions of the voltages are drawn in their effectiveness and the output voltage is inversed in relation to the input voltage.

Due to the fact that the voltage across C1 is always nearly equal to the input voltage, the voltage stress of the active switch is equal to the output voltage

$$U_S = U_2 \ . \tag{4}$$

The voltage stress across the diodes is also the same

$$U_{D1} = U_{D2} = -U_2 \ . \tag{5}$$

Summarizing one can say that the voltage stress of the semiconductors is equal to the one of the classical Boost converter.

The disadvantage of this concept is the abrupt charging of the capacitor C1, which also stresses the input source U1, the diode D1, and the electronic switch S1. When the switch S1 is turned off, the capacitor C1 is discharged by the current through L1. Therefore, the voltage decreases by Δu_{C1}. When S1 is turned on again, D1 turns on, too, and charges the capacitor up to the input voltage. Summarizing all parasitic resistors (from the electronic switch S1, the diode D1, the capacitor C1, and the wiring) in this loop together into R, and modelling the diode by a knee-voltage VD and the differential resistor RD one can write for this charging current according to Kirchhoff's voltage law

$$U_1 = Ri + V_D + \frac{1}{C_1}\int_0^t i dt + (U_1 - \Delta u_{C1}) \qquad \Delta u_{C1} - V_D = Ri + \frac{1}{C_1}\int_0^t i dt \ . \tag{6}$$

Laplace transformation leads to

$$\frac{\Delta u_{C1} - V_D}{s} = R \cdot I(s) + \frac{1}{C_1} \cdot \frac{1}{s} \cdot I(s) \ . \tag{7}$$

Back transformation leads to the exponential current form

$$i(t) = \frac{\Delta u_{C1} - V_D}{R} \exp\left(-\frac{1}{C_1 \cdot R} t\right) \ . \tag{8}$$

One has to keep in mind that this current flows, additional to the current through L1, out of the input source and stresses also the active switch. The peak-value of this additional current is

$$\hat{I} = \frac{\Delta u_{C1} - V_D}{R} \tag{9}$$

and decreases with the time constant

$$\tau = C_1 \cdot R \ . \tag{10}$$

This process should end within the on-time of the active switch. The minimal on-time of the active switch should therefore be about five-times the time-constant τ

$$T_{on,\min} = 5 \cdot \tau = 5 \cdot C_1 \cdot R \, . \tag{11}$$

This exponential current leads not only to an additional peak current stress, but also to additional losses. On the assumption that the minimal on-time of the switch is equal or larger than five times the time constant, one can write for the energy which is transferred into heat during one cycle (there is only a negligible error, when infinity is taken for the upper limit in the integral)

$$W_R = \int_0^\infty u_R i dt = \int_0^\infty R i^2 dt = \int_0^\infty R \frac{(\Delta u_{C1} - V_D)^2}{R^2} \exp\left(-\frac{2}{C_1 \cdot R} t\right) dt \ . \tag{12}$$

This leads to an additional loss energy per cycle

$$W_R = \frac{C_1 \cdot (\Delta u_{C1} - V_D)^2}{2} \, . \tag{13}$$

The loss is distributed across the parasitic resistances in the charging loop and depends on the switching frequency according to

$$P_R = f \frac{C_1 \cdot (\Delta u_{C1} - V_D)^2}{2} \, . \tag{14}$$

Please keep in mind that this loss occurs independently of the value of the resistor! In the result the resistor does not occur. Even when one uses the best available components, or even ideal components, this loss occurs and no improvement is achieved!

With these findings we can define the limits of the resistor R, so that the maximum current is lower than a chosen maximum value $\hat{I}$

$$R \geq \frac{\Delta u_{C1} - V_D}{\hat{I}} \ . \tag{15}$$

On the other side the resistor must be lower than

$$R \leq \frac{T_{on,\min}}{5 \cdot C_1} \ , \tag{16}$$

so that the capacitor can be charged up completely. To reduce the peak current, a discrete resistor which supplements the parasitic resistors can be used without reducing the efficiency.

3. Improvement of the converter

3.1 Basics

In this chapter an improvement of the converter which has no additional losses (when ideal devices could be used) is treated. The circuit is shown in Fig. 2, an inductor L2 is connected in series to D1.

When the active switch S1 is turned on, a loop according to the differential-integral equation occurs

$$U_1 = L_2 \frac{di}{dt} + Ri + V_D + \frac{1}{C_1} \int_0^t i dt + (U_1 - \Delta u_{C1}) \qquad \Delta u_{C1} - V_D = L_2 \frac{di}{dt} + Ri + \frac{1}{C_1} \int_0^t i dt \ . \tag{17}$$

In the resistor R all parasitic resistors of the loop are subsumed. Laplace transformation leads to

$$\frac{\Delta u_{C1} - V_D}{s} = L_2 \cdot s \cdot I(s) + R \cdot I(s) + \frac{1}{C_1} \cdot \frac{1}{s} \cdot I(s) \, . \tag{18}$$

Now the charging current takes place as a damped harmonic ringing

$$i(t) = \frac{\Delta u_{C1} - V_D}{L_2 \sqrt{\frac{1}{C_1 L_2} - \frac{R^2}{4L_2^2}}} \exp\left(-\frac{R}{2L_2}\right) \sin\left(\sqrt{\frac{1}{C_1 L_2} - \frac{R^2}{4L_2^2}}\, t\right) . \tag{19}$$

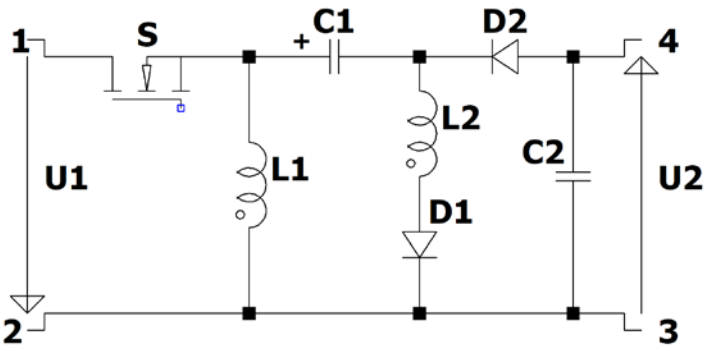

Fig. 2 Improved converter.

This ringing stops, when the current reaches zero after the first half-period. For dimensioning the converter one can neglect the losses. The ringing can now be simplified to a harmonic oscillation according to

$$i(t) = (\Delta u_{C1}) \sqrt{\frac{C_1}{L_2}} \sin\left(\sqrt{\frac{1}{C_1 L_2}}\, t\right) . \tag{20}$$

The amplitude of the charging current is therefore

$$\hat{I} = \Delta u_{C1} \sqrt{\frac{C_1}{L_2}} . \tag{21}$$

The period T of this oscillation can be calculated from

$$\omega = 2\pi f = \frac{2\pi}{T} = \sqrt{\frac{1}{C_1 L_2}} . \tag{23}$$

The current reaches zero after a half-period and the diode D1 turns off. This leads to the necessary minimal on-time according to

$$T_{on,\min} = \pi \sqrt{C_1 L_2} . \tag{24}$$

3.2 Dimensioning

The converter is an inverting step-up converter. If step-up ratios higher than two-times are desired, the duty cycle must be higher than 0.5. Half of the switching period can be used for the charging of C1. The output capacitor C2 has to supply the load during the on-time of the active switch. During this time the voltage across C2 is decreasing by

$$\Delta u_{C2} = \frac{1}{C_2} \int_0^{d \cdot T} I_{LOAD} dt = \frac{I_{LOAD} \cdot d \cdot T}{C_2} . \tag{25}$$

Using the switching frequency f instead of the switching period T, one gets for the capacitor the equation

$$C_2 = \frac{I_{LOAD} \cdot d}{\Delta u_{C2} \cdot f} . \tag{26}$$

Substituting the duty cycle by

$$d = \frac{U_2 - U_1}{U_2} \ , \tag{27}$$

one gets the dimensioning equation for the output capacitor C2 according to

$$C_2 \geq \frac{U_2 - U_1}{U_2} \cdot \frac{I_{LOAD}}{\Delta u_{C2} \cdot f} \ . \tag{28}$$

To compensate the influence of the parasitic resistor of C2, a capacitor value of about two-times will be used. The converter coil L1 can be calculated as in a normal Boost converter. During the on-time of the active switch, the input voltage lies across the inductor L1, and the current increases by ΔI_{L1}

$$U_1 = L_1 \frac{\Delta I_{L1}}{d \cdot T} \ . \tag{29}$$

Inserting again the duty cycle one gets the dimensioning equation according to

$$L_1 = \frac{U_1 \cdot d \cdot T}{\Delta I_{L1}} = \frac{U_2 - U_1}{U_2} \cdot \frac{U_1}{\Delta I_{L1} f} \ . \tag{30}$$

Now one has to dimension the resonance circuit. C1 cannot be chosen too large, as the recharge has to end within the on-time of the active switch. During the off-time of the active switch the current flowing through the coil L1 flows also through C1 and the voltage across it is reduced by

$$\Delta u_{C1} = \frac{1}{C_1} \int_{d \cdot T}^{T} \bar{I}_{L1} dt = \frac{\bar{I}_{L1} \cdot (1-d) \cdot T}{C_1} \ . \tag{31}$$

The mean value $\bar{I}_{L1}$ of the current through L1 can be calculated by the charge balance across C2 (in steady-state the current through a capacitor has to be zero in the mean)

$$I_{LOAD} \cdot d = \left(\bar{I}_{L1} - I_{LOAD} \right) (1-d) \ . \tag{32}$$

This leads to

$$\bar{I}_{L1} = \frac{I_{LOAD}}{1-d} \ . \tag{33}$$

The capacitor can therefore be dimensioned according to

$$C_1 = \frac{I_{LOAD}}{\Delta u_{C1} \cdot f} \ . \tag{34}$$

The resonance coil L2 has to be dimensioned for the minimal on-time and leads to the inequation

$$L_2 \leq \frac{T_{on,\min}^2}{\pi^2 C_1} \ . \tag{35}$$

By choosing the maximum amplitude of the recharging current, a second inequation can be found according to

$$L_2 \geq \frac{(\Delta u_{C1})^2 C_1}{\hat{I}^2} \ . \tag{36}$$

Fig. 3 shows the difference in the input current of the original circuit according to Fig. 1 and the improved converter according to Fig. 2 with the same current scale. The difference can be easily seen. As shown above, one can reduce the peak current without a reduction of the efficiency (also proved above) by inserting a resistor in series to the diode D1. This resistor would not only damp the current, but also reduce the electromagnetic disturbance. But using the resonance circuit (Fig. 3.b) to recharge the capacitor improves the efficiency and reduces the electromagnetic disturbance much more, due to a slower derivative of the current.

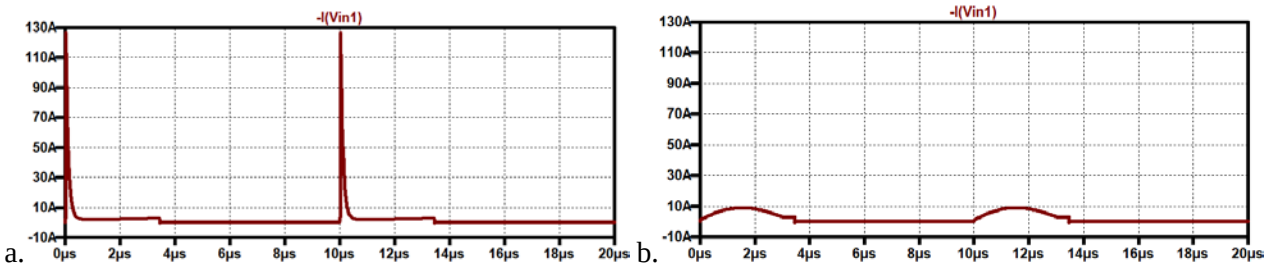

Fig. 3. Input current according to the converter: (a) Fig. 1, (b) Fig. 2, [7].

3.3 Improvement of the input current

The current flowing into the original converter (Fig. 1) and into the new one (Fig. 2) is pulsating. If this has to be reduced, e.g. for EMC-reasons or for reducing the input capacitor, the position of the capacitor C2 can be changed. Instead of connecting it between the output connectors, it can be connected between the positive input and the negative output connectors as shown in Fig. 4.

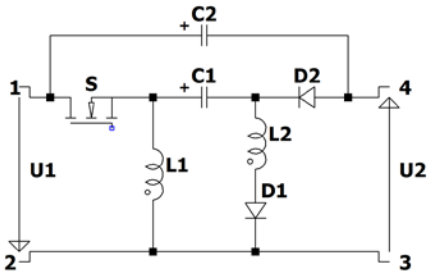

Fig. 4 Converter with storage capacitor between in- and output.

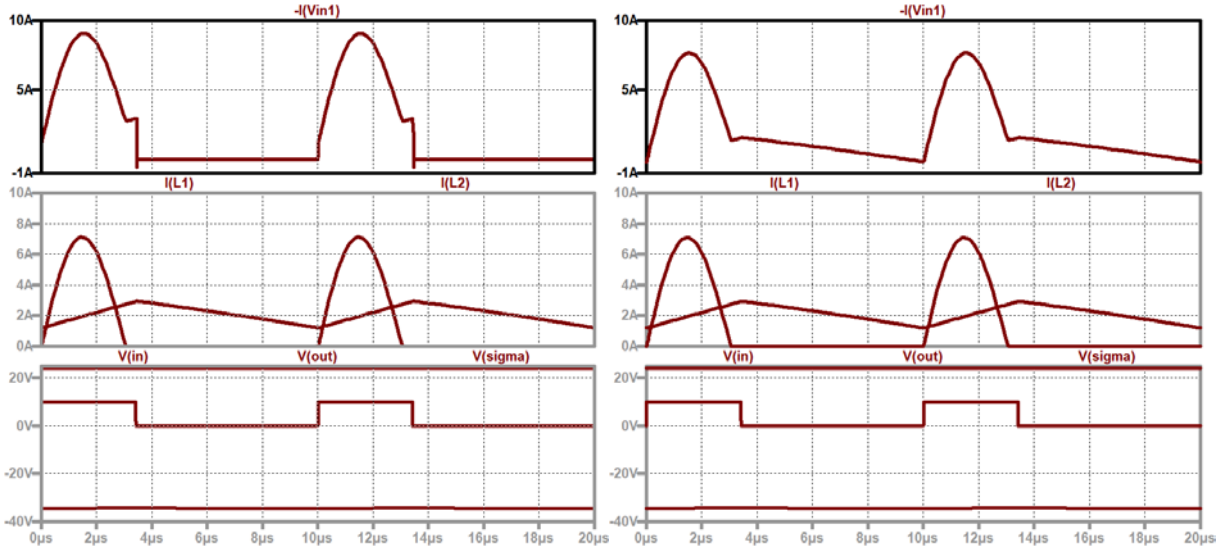

Fig. 5 (up to down): input current; current through the coils; input voltage, control signal, output voltage according to converter: (a) Fig. 2, (b) Fig. 4, [7].

Fig. 5 shows the input current, the currents through the inductors, and in the last graph the input voltage, the control signal, and the output voltage of the converters according to Fig. 2 and Fig. 4. The scales are the same. The difference lies in the input current. The current through the inductors are trapezoid through the main inductor L1 and sinusoidal through L2. In the converter with C2 in parallel to the output terminals, the input current is the sum of both currents through the two coils during mode M1 and zero during mode M2. The input current is therefore pulsating. When the capacitor C2 is connected between input and output, a continuous input current occurs and the maximum value is reduced. Furthermore, there are no steps in the input current which reduce electromagnetic disturbances.
Another interesting fact is that the converter has no inrush current compared to other boost converter topologies. This advantage is caused by the fact that the electronic switch is in series to the input voltage and no current can flow into the circuit, when the power source is applied to the converter (naturally the electronic switch must be turned off). To charge the capacitor a soft-start (increasing slowly the duty cycle until the desired voltage is reached) must be carried out.
It should be mentioned that the converter works also well in the discontinuous mode.

4. Dynamics of the inverting improved super lift Luo converter

4.1 Idealized model

During mode M1 (Fig. 6.a) the electronic switch S is on and the diode D2 is off. D1 conducts only at the beginning and turns off, when the current through L2 reaches zero. The capacitor C2 supplies the load. Diode D1 is conducting until C1 is charged to the input voltage (or a little bit higher, when the resonance circuit is only low damped; for ideal components the capacitor would charge up to $U1+\Delta u_{C1}$). For the dynamics C1, L2 and D1 can be neglected, because the voltage across C1 is always nearly equal to about the input voltage U1, and the current through L2 reaches zero during the on-time of the electronic switch S. Therefore, only two state equations are necessary to describe the dynamics.

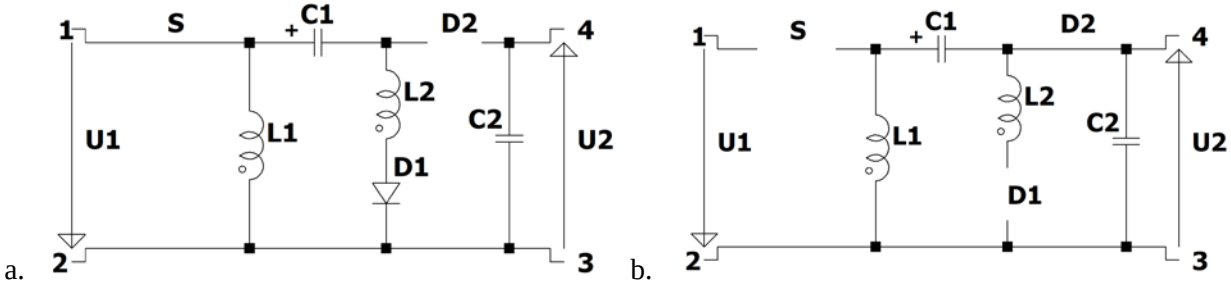

Fig. 6 Equivalent circuit during mode M1 (a) and M2 (b).

The state equations during M1 are

$$\frac{di_{L1}}{dt}=\frac{u_1}{L_1}, \qquad \frac{du_{C2}}{dt}=\frac{-u_{C2}/R}{C_2} . \tag{37}$$

In mode M2 (only diode D_2 is conducting) the voltage across C1 is the input voltage and as this voltage can have changed in the next cycle, we write a small letter to show that this input function is a time variable. Now one can write

$$\frac{di_{L1}}{dt}=\frac{u_1-u_{C2}}{L_1}, \qquad \frac{du_{C2}}{dt}=\frac{i_{L1}-u_{C2}/R}{C_2} . \tag{38}$$

Combining these equations with the help of the state-space averaging method leads to

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} 0 & \frac{d-1}{L_1} \\ \frac{1-d}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} (u_1) \ . \tag{39}$$

Linearizing this nonlinear differential equation results in

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & \frac{D_0-1}{L_1} \\ \frac{1-D_0}{C_2} & -\frac{1}{C_2 R} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & -\frac{I_{L10}}{C_2} \end{bmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix} \ . \tag{40}$$

The stationary equations for the operating point can be written according to

$$(D_0 - 1) U_{C20} + U_{10} = 0 \tag{41}$$

$$(1 - D_0) I_{L10} - U_{C20} / R = 0 \tag{42}$$

leading to the operating point values of the improved converter according to

$$U_{C20} = \frac{1}{1-D_0} U_{10}, \tag{43}$$

$$I_{L10} = \frac{U_{C20}}{R} \frac{1}{1-D_0} = \frac{I_{LOAD}}{1-D_0} \ . \tag{44}$$

Now one can Laplace transform the linearized differential equation according to

$$\begin{bmatrix} s & \frac{1-D_0}{L_1} \\ -\frac{1-D_0}{C_2} & s + \frac{1}{RC_2} \end{bmatrix} \begin{pmatrix} I_{L1}(s) \\ U_{C2}(s) \end{pmatrix} = \begin{bmatrix} \frac{1}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & -\frac{I_{L10}}{C_2} \end{bmatrix} \begin{pmatrix} U_1(s) \\ D(s) \end{pmatrix} \ . \tag{45}$$

For shorter calculation one can use abbreviations for the elements of the state and of the input matrixes

$$\begin{bmatrix} s & -A_{12} \\ -A_{21} & s - A_{22} \end{bmatrix} \begin{pmatrix} I_{L1}(s) \\ U_{C2}(s) \end{pmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ 0 & B_{22} \end{bmatrix} \begin{pmatrix} U_1(s) \\ D(s) \end{pmatrix}. \tag{46}$$

Using Crammer's law one can easily calculate the transfer functions. For the denominator one has to calculate the determinant of the coefficient matrix

$$Den = \begin{vmatrix} s & -A_{12} \\ -A_{21} & s - A_{22} \end{vmatrix} = s^2 - A_{22} s - A_{12} A_{22} \ . \tag{47}$$

The poles can be calculated according to

$$s_{1,2} = +\frac{A_{22}}{2} \pm \sqrt{\left(\frac{A_{22}}{2}\right)^2 + A_{12} A_{21}} \ . \tag{48}$$

The term under the root is negative and the poles are therefore conjugate complex. The imaginary part shows the angular frequency of the poles and the damping is given by the real part.
One can calculate four transfer functions. The numerator is for $U_{C2}(s)/D(s)$,

$$NumU2D = \begin{vmatrix} s & B_{12} \\ -A_{21} & B_{22} \end{vmatrix} = B_{22} s + A_{21} B_{12}, \tag{49}$$

this transfer function shows a non-phase minimum behaviour. Fig. 7 shows a DC gain of 150, a sharp resonance at 500 Hz (a larger output capacitor with 330 µF is used for the Bode plots: for a smaller capacitor e.g. 47 µF the resonance is shifted to 1350 Hz). The influence of the positive zero starts at a ten-time higher frequency than the resonance. So the influence is marginal. The zero is on the right side of the complex plane. The larger the inductor the nearer the zero to the ordinate and the larger the influence of the non-phase minimum behaviour. The capacitors do not influence the position of the zero, only the operating point and the main inductor L1 influence it. The zero of the transfer function between the output voltage and the duty cycle is given by

$$-\frac{I_{L10}}{C_2}s+\frac{U_{C20}(1-D_0)}{L_1C_2}=0 \qquad s_Z=+\frac{U_{C20}(1-D_0)}{I_{L10}L_1} \tag{50}$$

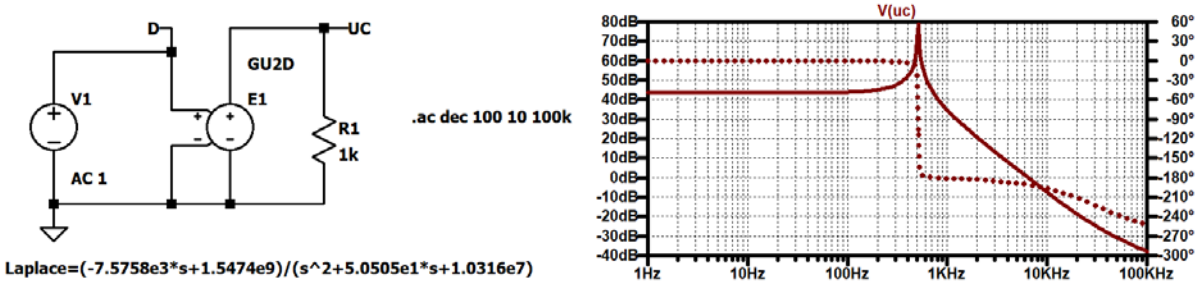

Fig.7 Bode diagram between output voltage and duty cycle (solid line: gain response, dotted line: phase response).

For $U_{C2}(s)/U_1(s)$, which describes the influence of the input voltage change to the output voltage one gets

$$NumU2U1=\begin{vmatrix} s & B_{11} \\ -A_{21} & 0 \end{vmatrix}=A_{21}B_{11}\ . \tag{51}$$

Fig. 8 shows the Bode diagram between the output voltage and the input voltage. This is a phase-minimum system. The phase jumps from zero to -180° at the resonance.

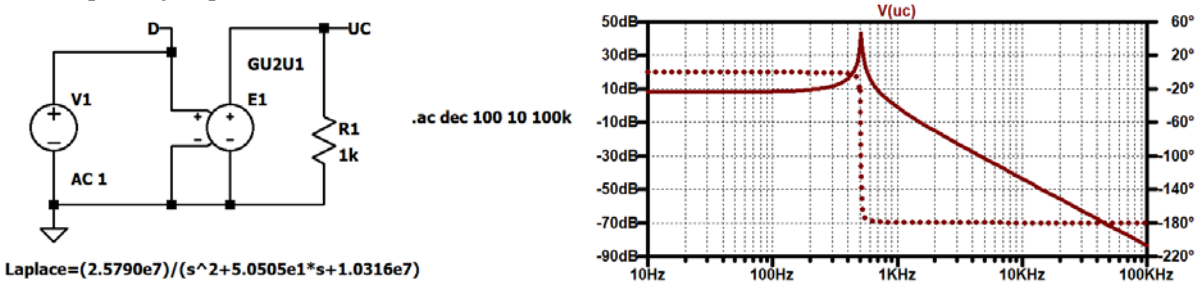

Fig. 8 Bode diagram between output voltage and input voltage (solid line: gain response, dotted line: phase response).

For the current one gets the numerator of IL(s)/D(s)

$$NumILD=\begin{vmatrix} B_{12} & -A_{12} \\ B_{22} & s-A_{22} \end{vmatrix}=B_{12}s+A_{12}B_{22}-A_{22}B_{12}\ . \tag{52}$$

The zero is on the left side of the complex plane, the phase tends therefore only to -90 degree (Fig. 9).

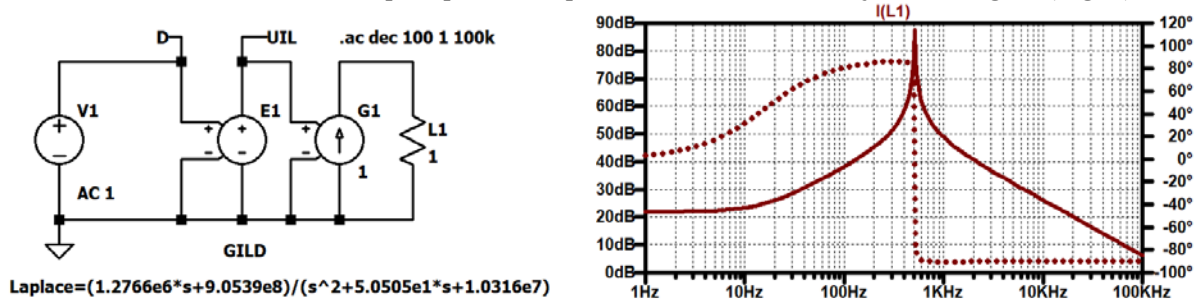

Fig 9 Bode diagram between inductor current and duty cycle (solid line: gain response, dotted line: phase response).

The numerator for IL(s)/U1(s) (the current in dependence of the input voltage) is

$$NumIU1 = \begin{vmatrix} B_{11} & -A_{12} \\ 0 & s - A_{22} \end{vmatrix} = B_{11}s - B_{11}A_{22}\,. \tag{53}$$

The zero is on the left side and shifts the phase by 90°. This is advantageous for the control of the current directly, or in a two-loop control with inner current loop.

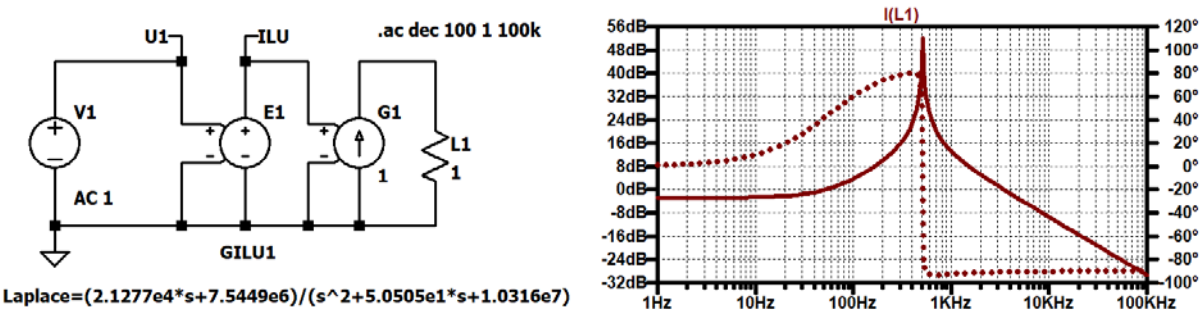

Fig. 10 Bode diagram between inductor current and input voltage (solid line: gain response, dotted line: phase response).

Now one can calculate the transfer functions. The transfer functions between output voltage and duty cycle and input voltage are

$$\frac{U_{C2}(s)}{D(s)} = \frac{-\frac{I_{L10}}{C_2}s + \frac{U_{C20}(1-D_0)}{L_1C_2}}{s^2 + s\frac{1}{RC_2} + \frac{(1-D_0)^2}{L_1C_2}}, \qquad \frac{U_{C2}(s)}{U_1(s)} = \frac{(1-D_0)}{L_1C_2}\frac{1}{s^2 + s\frac{1}{RC_2} + \frac{(1-D_0)^2}{L_1C_2}} \tag{54, 55}$$

and the transfer functions between current and duty cycle and input voltage can be written according to

$$\frac{I_{L1}(s)}{D(s)} = \frac{\frac{U_{C20}}{L_1}s + \left(\frac{U_{C20}}{L_1C_2R} + \frac{I_{L10}(1-D_0)}{L_1C_2}\right)}{s^2 + s\frac{1}{RC_2} + \frac{(1-D_0)^2}{L_1C_2}}, \qquad \frac{I_{L1}(s)}{U_1(s)} = \frac{\frac{1}{L_1}s + \frac{1}{L_1C_2R}}{s^2 + s\frac{1}{RC_2} + \frac{(1-D_0)^2}{L_1C_2}} \tag{56, 57}$$

The position of the poles is

$$s_{P1,2} = -\frac{1}{2RC_2} \pm \sqrt{\left(\frac{1}{2RC_2}\right)^2 - \frac{(1-D_0)^2}{L_1C_2}}\,. \tag{58}$$

4.2 Model with losses

The parasitic resistors and the knee-voltage of the diode V_D are included. The state equations during M1 are

$$\frac{di_{L1}}{dt} = \frac{1}{L_1}\{u_1 - (R_{L1} + R_S)i_{L1}\} \tag{59}$$

$$\frac{du_{C2}}{dt} = \frac{-u_{C2}}{C_2(R + R_{C2})}\,. \tag{60}$$

During M2 we have

$$\frac{di_{L1}}{dt}=\frac{1}{L_1}\left\{+u_1-(R_{C1}+R_{D2}+R_{L1}+R//R_{C2})i_{L1}-u_{C2}\frac{R}{R+R_{C2}}-V_D\right\} \tag{61}$$

With

$$i_{C2}=\frac{Ri_{L1}-u_{C2}}{R+R_{C2}} \tag{62}$$

one gets for the state equations

$$\frac{di_{L1}}{dt}=\frac{1}{L_1}\{+u_1-(R_{C1}+R_{D2}+R_{L1})i_{L1}-V_{D2}-u_{C2}-R_{C2}i_{C2}\} \tag{63}$$

$$\frac{du_{C2}}{dt}=\frac{Ri_{L1}-u_{C2}}{C_2(R+R_{C2})}\ . \tag{64}$$

$$\frac{d}{dt}\begin{pmatrix}i_{L1}\\u_{C1}\end{pmatrix}=\begin{bmatrix}\frac{R_{L1}+R_S d+(R_{C1}+R_{D2}+R//R_{C2})(1-d)}{L_1} & \frac{(d-1)R}{L_1(R+R_{C2})}\\ \frac{R}{C_2(R+R_{C2})} & -\frac{1}{C_2(R+R_{C2})}\end{bmatrix}\begin{pmatrix}i_{L1}\\u_{C1}\end{pmatrix}+\begin{bmatrix}\frac{1}{L_1}\\0\end{bmatrix}(u_1)+\begin{pmatrix}\frac{V_D(d-1)}{L_1}\\0\end{pmatrix}. \tag{65}$$

4.3 Dynamics simulation

Fig. 11 shows the nonlinear model according to Eq. (65). The derivatives are given by currents produced by the arbitrary current sources B1 for the current through L1 and B4 for the voltage across C2. The integration is done by 1 F capacitors. The 10 MΩ resistor in parallel has only stabilizing reasons and does not influence the result. To achieve a current as result, the voltage across C1 is fed to a voltage controlled current source G1. The current through the resistor named L1 corresponds to the current through L1. The input voltage and the duty cycle are produced by the piecewise linear voltage sources V1 and V3.

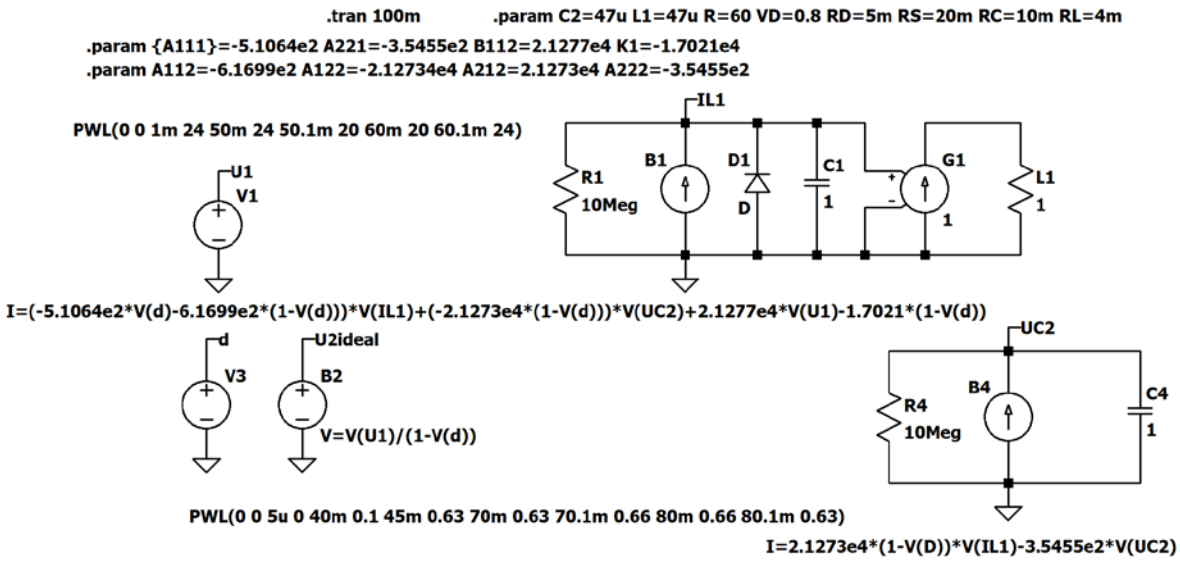

Fig. 11 Nonlinear model with losses included .

Fig. 12 shows the simulation circuit. The control signal is generated by the comparator U1, which compares the saw tooth signal generated by the voltage source V6 with the duty cycle produced by the voltage source V1. The active switch is a high-side one, therefore an isolated driver is necessary. The comparator is supplied only

by plus and minus 5 V, so the output signal has to be amplified. This is done by the voltage-controlled voltage source E1.

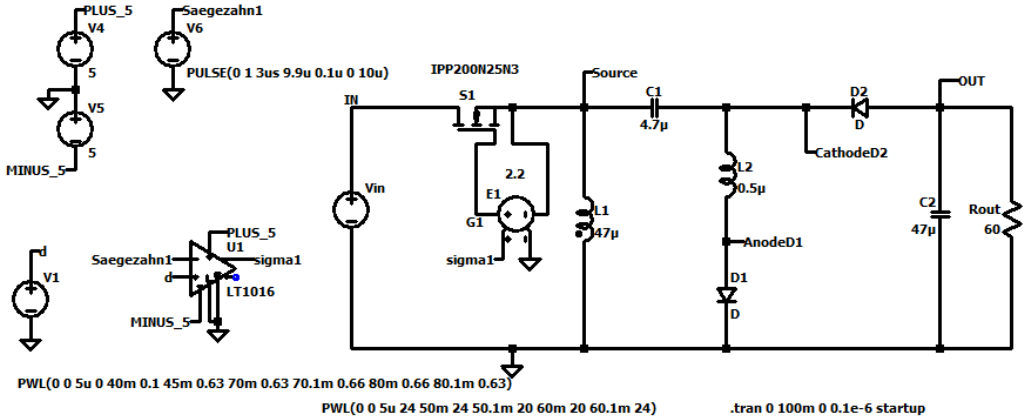

Fig. 12 Circuit simulation.

Fig. 13 shows the results. The duty cycle increases to obtain a soft-start of the converter. At 50 ms the input voltage makes a step down and after 10 ms the input voltage steps back. At 70 ms the duty cycle is stepped up and after 10 ms the duty cycle steps down to the previous value. The calculation with the model shows only the mean values of the voltage and the current, but represents the dynamic behavior very fast and quite precisely. The circuit simulation needs much more time for calculation and shows the ripple of the current (the broad red band in Fig.13.b). For the study of the dynamic behavior this is not really necessary.

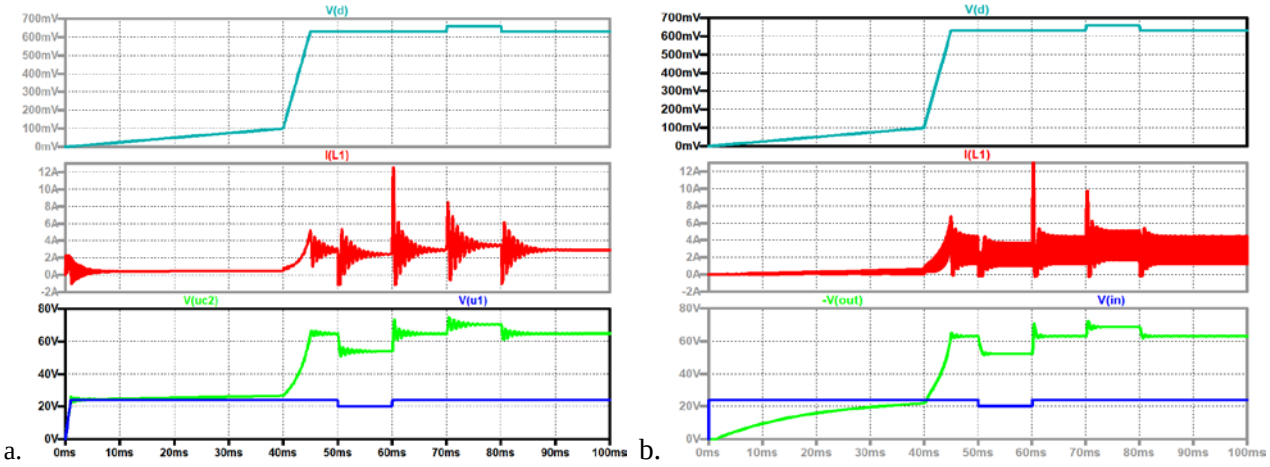

Fig. 13 Start-up, input voltage steps, duty cycle steps, up to down: duty cycle (turquoise); current through L1 (red), input voltage (blue), negative output voltage (green), (a) nonlinear model, (b) circuit simulation.

4.4 Feedforward control

The converter can be forward-controlled by a simple control law. With this feedforward control input changes can easily and faster be compensated. The control law can be derived directly from the voltage transformation

ratio. For a desired reference value U_2^* one can calculate the necessary duty cycle d in dependence on the input voltage U1 according to

$$d = \frac{U_2^* - U_1}{U_2^*} \quad . \tag{66}$$

One has to keep in mind, however, that this control law is derived from the ideal voltage transformation ratio which leads to a small error of the output voltage. One can calculate a more complicated control law by including the parasitic elements of the converter; but still this law is deficient, due to the fact that the components have tolerances, change their values depending on the temperature, and also change by aging. Therefore, it is recommendable to combine the simple control law by a feedback controller which has only to compensate the error of the forward control. Fig. 14 depicts the circuit used for the simulation. The control law is calculated by the arbitrary voltage source B1. The reference value is generated by the piece-wise linear voltage source V2. Fig. 14 shows also current i(L1), the input, the output voltages, and the voltage across C1.

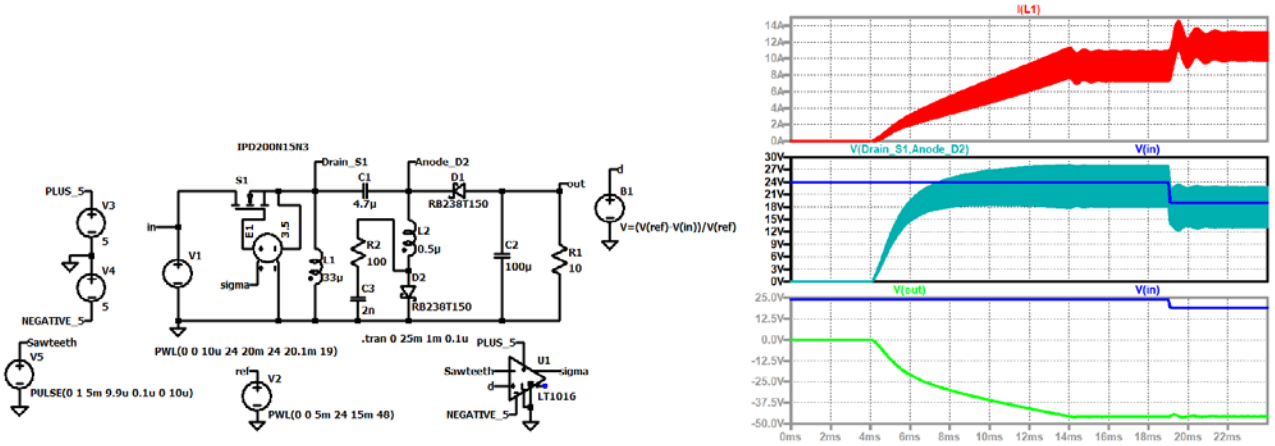

Fig. 14 Feedforward control: circuit simulation and up to down: current through L1 (red); input voltage (blue), voltage across C1 (turquoise); input voltage (blue), output voltage (green).

4.5 Measurement of the function

Fig. 15 shows the input current and the currents through the coils.

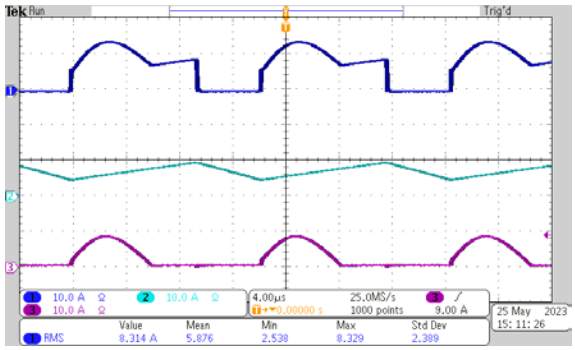

Fig. 15 up to down: input current (channel 1), current through L1 (channel 2), current through L2 (channel 3).

5. Conclusions

The improved negative output super-lift boost converter has several interesting features:

- Inverts the input voltage
- Same transformation ratio as the classical Boost converter
- Has no inrush current
- Start-up can be easily achieved by slowly increasing the duty cycle
- Combined with a positive output converter it can be used as supply for an inverter

Combined with a feedforward control it can be used for solar applications and for e-mobility to produce a negative output voltage.

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Felix A. Himmelstoss was born in 1956 in Moedling, Austria. He received the Dipl.-Ing. and Dr. (PhD) degrees from Technical University of Vienna, in 1981 and 1990, respectively. Since 1982 he has been working on different projects for Austrian companies developing power supplies and electrical drives. He is author of numerous technical and scientific papers and patents. His main research interests are converter topologies and their control. Dr. Himmelstoss is professor and program director emeritus of the Master Course Power Electronics of the University of Applied Sciences Technikum Wien.

Gabriel Hochmeister was born in 1996 in Moedling, Austria. He received the BSc in Electrical Engineering and the MSc in Power Electronics from the University of Applied Sciences Technikum Wien, in 2021 and 2023, respectively.

Dominik Petrovic was born in 1997 in Vienna, Austria. He received the BSc in Electrical Engineering and the MSc in Power Electronics from the University of Applied Sciences Technikum Wien, in 2021 and 2023, respectively.