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An incipient low cost cascaded transformer multilevel inverter topology utilizing minimum number of components with modified selective harmonic elimination modulation

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Abstract
In this paper, a novel cascaded transformer multilevel inverter is proposed. The number of the switching contrivances is reduced in the proposed topology. This topology comprises of a DC source, several single phase low-frequency transformers, two main power switches and some bidirectional switching contrivances. In this topology, only one bidirectional switch is employed for each transformer. However, in conventional cascaded transformer multilevel inverter, four switching contrivances are required for each transformer. Therefore, more output voltage levels can be obtained utilizing fewer switching components. Reduction in the number of switching contrivances which additionally betokens reduction in the number of gate drivers results in more minute size and low implementation cost. Switching power losses are withal reduced in this topology. Selective harmonic elimination (SHE) technique is applied to the proposed inverter to obtain a high quality output voltage. Simulation and experimental results are withal provided to verify the feasibility of the proposed converter.

Keywords: *Cascaded transformers multilevel inverter; Reduced number of switching devices, Selective harmonic elimination*

1. Introduction

During the past few years, multilevel inverters have played a major role in most systems such as immensely colossal motor drives, flexible AC transmission systems, power quality amelioration contrivances and renewable energy converters [1], [2] and [3]. Therefore, multilevel inverters have magnetized great attention of potency electronic engineers. Multilevel inverters benefit from sundry advantages such as lower switching losses, stepwise output voltage, more diminutive mundane mode voltage and lower peak inverse voltage (PIV) on switches [4], [5] and [6]. These advantages make multilevel inverters auspicious for many industrial applications. There are primarily three multilevel converter topologies soi-disant diode-clamped [7], flying capacitor [8] and cascaded H-bridge with separate DC sources [9]. They provide stepwise voltage with high quality. However, their main disadvantage, which is the extortionate number of switching components, restrains their applications. In diode-clamped configuration, regulating the capacitors voltages makes the control scheme intricate. Withal, abundant numbers of clamping diodes are required in this topology. Ladder structure of capacitors is utilized in flying capacitor multilevel inverters. Therefore the volume of the system is enlarged for the indispensability of more capacitors. Cascaded H-bridge structure has the advantage of being modular which makes this structure facilely expandable for higher number of output voltage levels. However, the desideratum for separate DC voltage sources for each module and the number of switching components are the main disadvantages for this configuration. For surmounting these quandaries, novel topologies of multilevel inverters are presented in recent years. The cascaded transformer multilevel topology is proposed [10] and [11]. This topology employs one single DC voltage source and several isolated low-frequency transformers. However, number of switching components is still to be reduced. In [12] and [13], incipient topologies are proposed in order to reduce the number of switches. Therefore, the main disadvantage of cascaded transformer inverter is that this topology has many switching components. Switching strategies of multilevel inverters are categorized into high switching frequency methods such as SPWM strategy [14] and low switching frequency

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techniques, often identically tantamount to fundamental switching frequency of the components, which engender stepwise output voltage waveform [15]. Second category comprises of three major switching strategies soi-disant optimized harmonic stepped waveform [16], selective harmonic mitigation PWM [17], and optimal minimization of the THD [18]. Selective harmonic elimination is as efficacious method to mitigate the low-order harmonic components. In this paper, a cascaded H-bridge reduced switch multilevel inverter is proposed which comprises of several low-frequency transformers. The number of switching components and gate drivers are minimized in this topology which reduced the size and the cost of entelechy. Selective harmonic elimination technique is employed to reach to a high quality output voltage. Simulation and experimental results designate the ability of the proposed topology in voltage engendering.

II. CASCADED TRANSFORMER H-BRIDGE MULTILEVEL INVERTER

In this section the traditional topology and two incipient topologies introduced for transformer predicated multilevel inverters are reviewed. Traditional cascaded H-bridge cells multilevel inverter needs several numbers of semiconductors and disunited DC sources, these several numbers of isolated sources and components are arduous to be provided and controlled so this is a solemn drawback for this topology. To eliminate desideratum for several isolated DC sources the cascaded transformer H-bridge multilevel was introduced in which the transformers are utilized in lieu of DC sources. Endeavoring reach to a less component topology and obtain an optimized topology have led to appear some incipient topology which utilize fewer semiconductors and DC sources. Cascaded transformer inverter with two DC sources (CTITS) is one of the most incipient less component topologies of transformer predicated multilevel inverter which have been introduced in [19]. Fig. 1a and b show traditional topology of cascaded transformer multilevel inverter and the CTITS respectively.

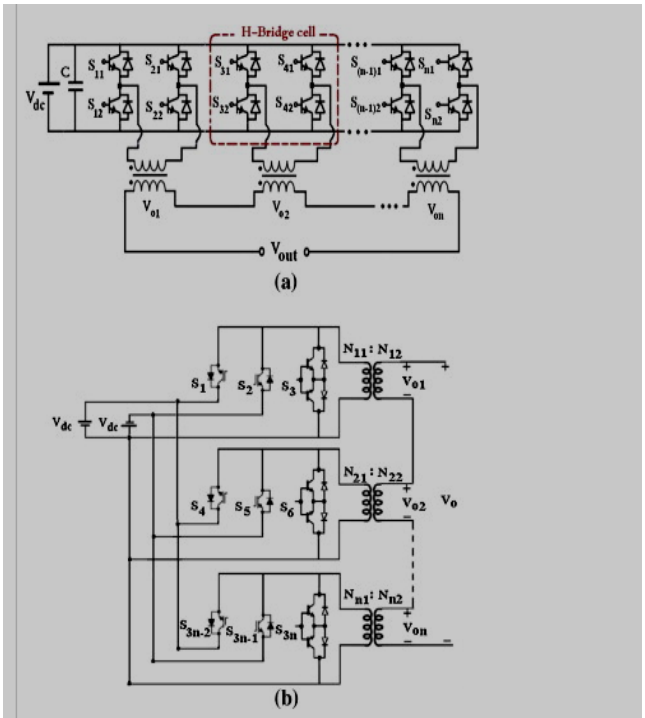


Figure 1.
(a) The traditional cascaded transformer multilevel inverter, (b) the CTITS topology.

III. PROPOSED INVERTER STRUCTURE

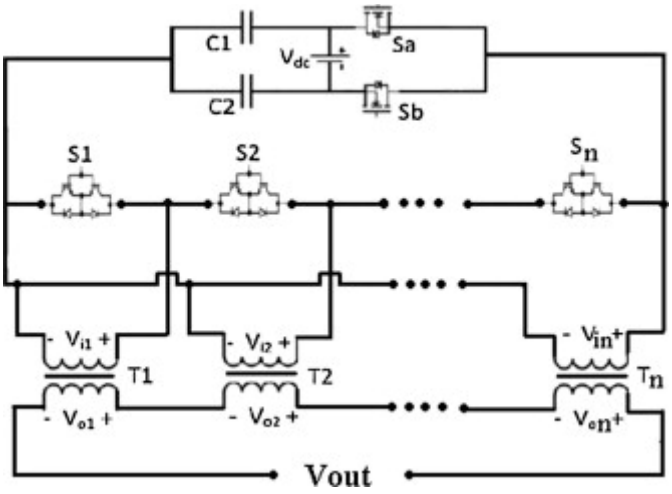
This topology consists of a DC voltage source and several single phase transformers. As it is shown in Fig. 2, two main switching contrivances are acclimated to transmute the polarity of the input voltage and for each transformer a bidirectional power switch is utilized. In comparison with the conventional cascaded H-bridge multilevel inverter, numbers of switching contrivances are decremented. Respectively, the numbers of the gate drivers are reduced. Compare to the traditional transformer predicated multilevel inverters, utilizing less switching contrivances as well as gate drivers in the proposed topology leads to cutting down in power losses, more diminutive size and low cost. In the proposed configuration, the number of switches required to obtain an m-level output voltage can be given as follows

$$SW=(m+1)$$

$$D = \frac{(m+3)}{2}$$

$$N = \frac{(m-1)}{2}$$

where *SW*, *D* and *N* are the number of the unidirectional switches, gate driver circuits and transformers respectively.



The secondary sides of the transformers are connected in series to synthesize the stepwise output voltage. The output phase voltage can be given by summing the output voltages of the transformers as below:

$$V_{on} = \frac{1}{a} V_{dc}$$

$$V_{out} = \frac{1}{a} \sum_{m=1}^{n} V_{om}$$

where V_{on}, *a*, V_{out} and *n* are the secondary voltage of each transformer, transformer ratio of transformers, output voltage of the inverter and number of cascaded transformers.

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