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CONTROL OF COMBINED KY AND BUCK-BOOST CONVERTER WITH COUPLED INDUCTOR

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Abstract
In this paper a voltage-boosting converter is presented, which combines one KY converter and one synchronously rectified buck-boost converter. The corresponding voltage gain is greater than that of the existing step-up converters. It overcomes all the disadvantage of older converter. It has added advantage such as its output terminal has got inductor thus making output free from ripples. More over its energy lost in the leakage inductor is replaced to the output capacitor. It also contains one charge pump and coupled inductor with turn's ratio. Since the proposed converter possesses an output inductor and output capacitor the output current is no pulsating and voltage is free from ripples. The proposed converter is first modeled with PI Controller. For better system dynamic performance converter is modeled with Fuzzy Logic Controller. The proposed converter gives output voltage of 72 V from 12 V DC. The fundamental output frequency was 50 Hz and the switching frequency was 100 kHz. The experiment result of two control methods shows that fuzzy control method needs much less time to reach steady state than that of PI control.
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Keywords: *Coupled inductor, Magnetizing inductor, Charge pump,Energy transferring capacitor.*

1. Introduction

This converter combines one KY converter, one traditional synchronously rectified (SR) buck-boost converter, and one coupled inductor with the turns ratio, which is used to improve the voltage gain. Therefore, the voltage gain is higher than that of the converter in and can be determined by adjusting both the duty cycle and the turns ratio. Moreover, the duty cycle and the turns ratio are independent, which means that tuning the duty cycle does not affect the turns ratio and vice versa. In addition, the proposed step-up converter has no floating output and has an output inductor; hence, the output current is non pulsating. Furthermore, part of the leakage inductance energy can be recycled to the output capacitor of the SR buck-boost converter. In this paper, a detailed description, along with some experimental results, is given to provide the effectiveness of the proposed converter.

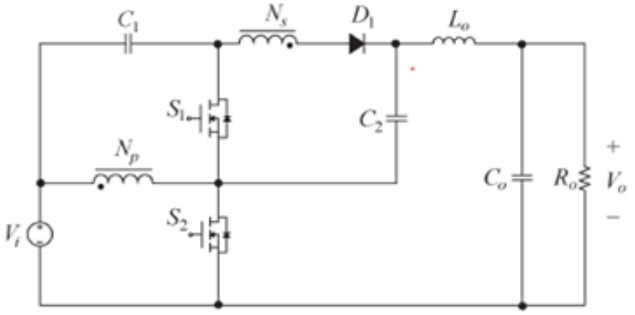

Fig.1. Proposed step-up converter

Fig.1. shows the proposed converter, which contains two MOSFET switches S_1 and S_2, one coupled inductor composed of the primary winding with N_p turns and the secondary winding with N_s turns, one energy-transferring capacitor C_1, one charge pump capacitor C_2, one diode D_1, one output inductor L_o, and one output capacitor C_o. In addition, the input voltage is denoted by V_i, the output voltage is

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signified by V_o, and the output resistor is represented by R_o.

Assumptions to be made are:

1) The coupled inductor is modeled as an ideal transformer except that one magnetizing inductor L_m is connected in parallel with the primary winding and one leakage inductor L_{l1} is connected in series with the primary winding. Therefore, coupling coefficient k is defined as $L_m/(L_m + L_{l1})$.
2) The proposed converter operates in the positive current mode. That is, the currents flowing through the magnetizing inductor L_m and the output inductor L_o are always positive.
3) The dead times between the two MOSFET switches are omitted. The MOSFET switches and the diodes are assumed to be ideal components.
4) The values of all the capacitors are large enough such that the voltages across them are kept constant at some values.
5) The magnitude of the switching ripple is negligible. Therefore, the small ripple approximation will be adopted herein in the analysis.

2. Basic Operating Principles

The following analysis contains the explanation of the power flow path for each mode, along with the corresponding equations and voltage gain. Inherently, there are two operating modes in the proposed converter. Moreover, the gate driving signals v_{gs1} and v_{gs2} of the two switches S_1 and S_2 have the duty cycles of $(1 - D)$ and D, respectively, where D is the dc quiescent duty cycle created from the controller. In addition, the input current is denoted by i_i, the current through the N_p winding is signified by i_{Np}, the current through the N_s winding is represented by i_{Ns}, the current through L_m is denoted by i_{Lm}, the current through L_o is indicated by i_{Lo}, and the current through R_o is signified by I_o. On the other hand, the voltage across L_m or the voltage across the N_p winding is signified by V_{Np}, the voltage across the N_s winding is represented by V_{Ns}, the voltage across C_1 is indicated by V_{C1}, the voltage across C_2 is denoted by V_{C2}, and the voltage across L_o is described by V_{Lo}.

Its operation is analyzed in two ways:

A. Voltage Gain Considering Coupling Coefficient Equal to One
B. Voltage Gain Considering Coupling Coefficient Not Equal to One

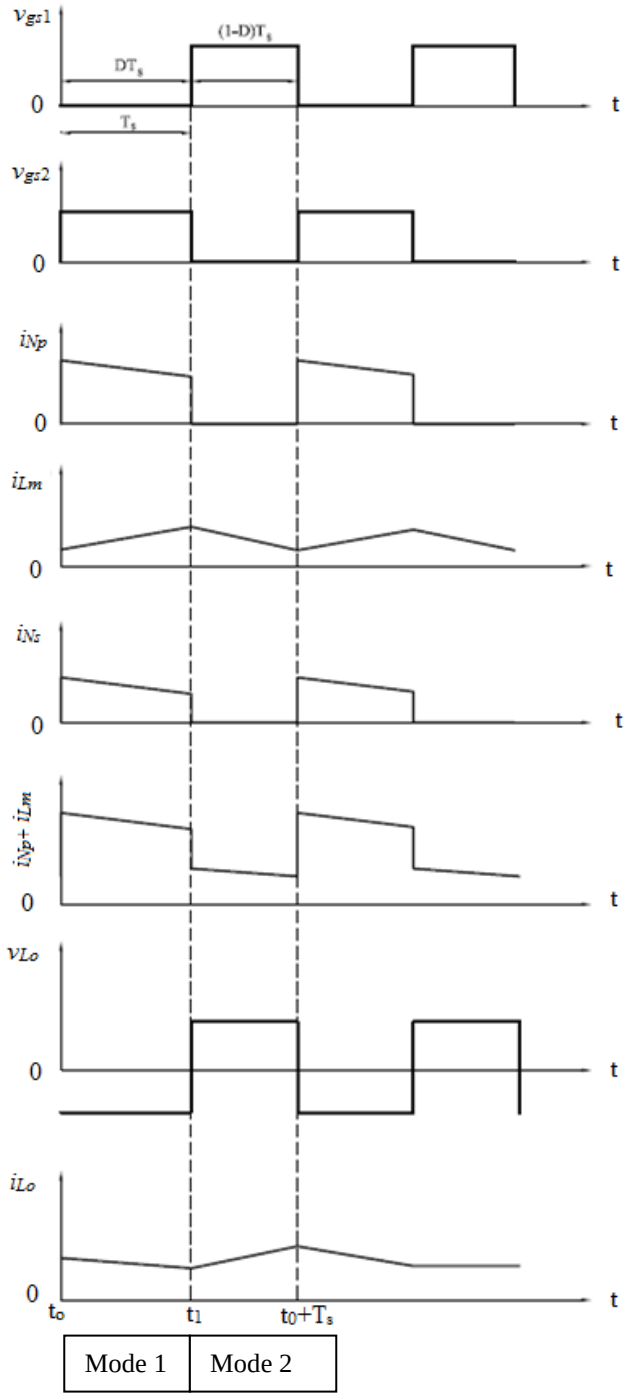

Fig.2. Key waveforms of the proposed converter.

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A. Voltage Gain Considering Coupling Coefficient Equal to One

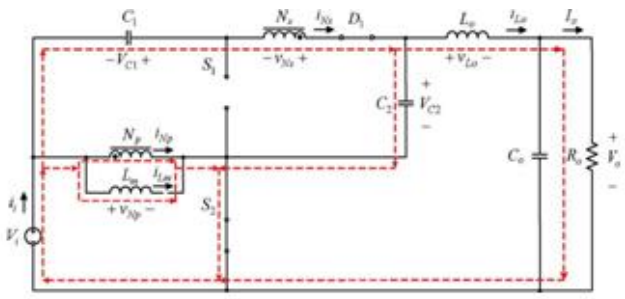

Fig.3. Power flow in mode 1 with coupling coefficient equal to one.

Mode 1: During this interval, as shown in Fig.3., S_1 is turned off but S_2 is turned on. Therefore, input voltage V_i is imposed on N_p, thus causing L_m to be magnetized and the voltage across N_s to be induced, equal to $V_i \times N_s/N_p$. In addition, D_1 becomes forward-biased; C_2 is charged to $V_i + V_{C1} + V_i \times N_s/N_p$; and the voltage across L_o, i.e., V_{Lo}, is a negative value, equal to $V_{C2} - V_o$, thus making L_o demagnetized. As a consequence, input voltage V_i, together with the voltage across C_1 (V_{C1}), plus the induced voltage on N_s (V_{Ns}), plus the voltage across L_o (V_{Lo}), provides the energy to the load. In addition, the associated equations are as follows:

$$V_{Np} = V_i \tag{1}$$

$$V_{Lo} = V_{C2} - V_o \tag{2}$$

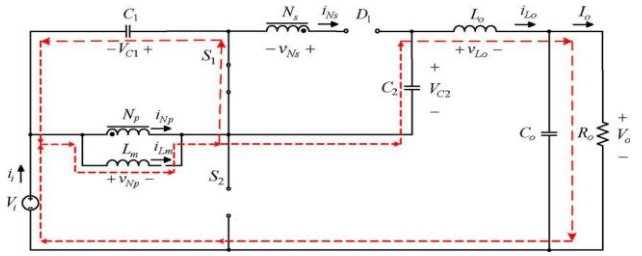

Fig.4. Power flow in mode 2 with coupling coefficient equal to one.

Mode 2: During this interval, as shown in Fig.4. S_1 is turned on but S_2 is turned off. Therefore, the $-V_{C1}$ voltage is imposed on N_p, thereby causing the magnetizing inductor L_m. to be demagnetized and the voltage across N_s to be induced, equal to $-V_{C1} \times N_s/N_p$. In addition, D_1 becomes reverse biased, the voltage on L_o is a positive value, equal to $V_i + V_{C1} + V_{C2} - V_o$, thus causing L_o to be magnetized. As a result, the input voltage V_i, together with the voltage across L_m(V_{Np}),plus the voltage across C_2 (V_{C2}), provides the energy to L_o and the load. In addition, the corresponding equations are as follows:

$$V_{Np} = -V_{C1} \tag{3}$$

$$V_{Lo} = V_i + V_{C1} + V_{C2} - V_o \tag{4}$$

By applying the voltage-second balance principle to L_m over one switching period, the following equation can be obtained:

$$V_i \times D + -V_{C1} \times 1 - D = 0 \tag{5}$$

In addition, by rearranging the above equation, the voltage across C_1, i.e., V_{C1}, can be obtained as follows:

$$V_{C1} = \frac{D}{1-D} \times V_i \tag{6}$$

Likewise, by applying the voltage-second balance principle to Lo over one switching period, the following equation can be obtained:

$$(V_{C2} - V_0) \times D + (V_i + V_{C1} + V_{C2} - V_0) \times (1 - D) = 0 \tag{7}$$

The voltage across C_2, i.e., V_{C2}, can be represented by

$$V_{C2} = V_i + V_{C1} + V_i \times \frac{N_s}{N_p} \tag{8}$$

Next, based on (6)–(8), the corresponding voltage gain can be expressed to be

$$\frac{V_0}{V_i} = \frac{2-D}{1-D} + \frac{N_s}{N_p} \tag{9}$$

From (9), it is shown that $0 < D < 1$.

B. Voltage Gain Considering Coupling Coefficient Not Equal to One

In this case, the coupling coefficient k is not equal to one, i.e., the leakage inductor L_{l1} is taken into account. Moreover, the operating modes are also the same as those mentioned in mode1 of previous case.

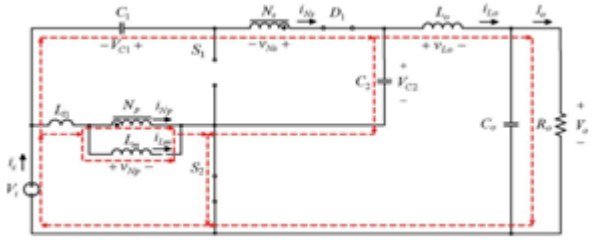

Fig.5. Power flow in mode 1 with coupling coefficient smaller than one.

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Mode 1: During this interval, as shown in Fig.5. the following equations, containing coupling coefficient k, can be obtained. At the same time, both L_m and L_{l1} are simultaneously magnetized. Hence, the corresponding equations are as follows

$$V_{Np} = \frac{L_m}{L_m + L_{l1}} \times V_i \quad (10)$$

$$V_{Ns} = V_{Np} \times \frac{N_S}{N_p} = kV_i \times \frac{N_S}{N_p} \quad (11)$$

In addition, the voltages on C_2 and L_o can be depicted as follows

$$V_{C2} = V_i + V_{C1} + V_{Ns} = Vi + V_{C1} + kV_i \times \frac{N_S}{N_p} \quad (12)$$

$$V_{Lo} = V_{C2} - Vo \quad (13)$$

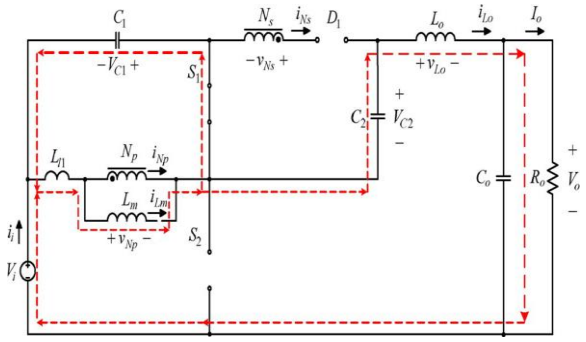

Fig.6. Power flow in mode 2 with coupling coefficient smaller than one.

Mode 2*:* During this interval, as shown in Fig.6. the voltages across L_o and C_1 are to be expressed as follows. Above all, part of the energy stored in L_m and L_{l1} can be transferred to C_1. Hence, the corresponding equations are

$$V_{Np} = -kV_{C1} \quad (14)$$

$$V_{Lo} = V_i + V_{C1} + V_{C2} - V_0 \quad (15)$$

By applying the voltage-second balance to both L_m and L_{l1} over one switching period, one can get

$$V_i \times D + -V_{C1} \times 1 - D = 0 \quad (16)$$

Sequentially, by rearranging the above equation, the voltage across C_1, i.e., V_{C1}, can be obtained to be

$$Vc_1 = \frac{D}{1-D} + \frac{Ns}{N_p} \quad (17)$$

Likewise, by applying the voltage-second balance principle to L_o over one switching period, the following equation can be obtained to be

$$Vc_2 - V_o \times D + Vi + Vc_1 + Vc_2 - V_0 \times 1 - D = 0 \quad (18)$$

Next, substituting (12) and (17) into (18) yields the voltage gain

$$\frac{V_0}{V_i} = \frac{2-D}{1-D} + \frac{Ns}{N_p} \quad (19)$$

From equation 19 it is clear that voltage gain can be changed by adjusting duty cycle and turns ratio independently. So this converter can achieve much higher gain than that of other converters.

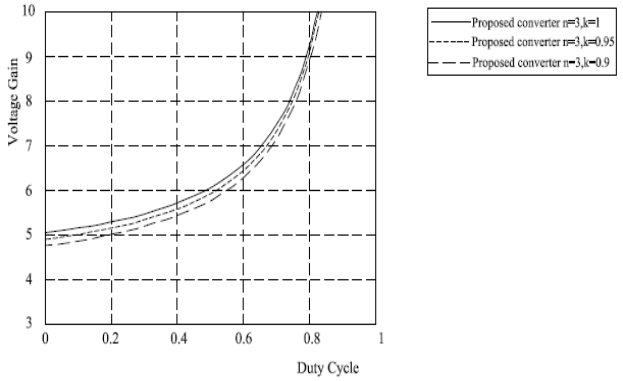

Fig.7. Curves of voltage gain versus duty cycle for the proposed converter with different values of coupling

Fig.7. shows the voltage gain verses duty cycle with same coefficient of coupling k and different turns ratio. We can see that as duty cycle increases gain increases and also as turns ratio n ($\frac{N_s}{N_p}$) increases gain increases.

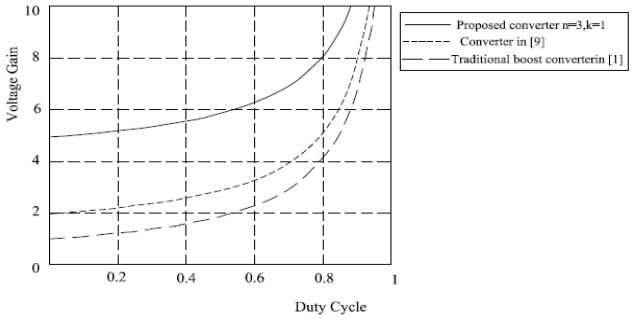

Fig.8. Comparison of voltage gain verses duty cycle for same turns ratio but different coupling coefficient

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Fig.8. shows voltage gain versus duty cycle for different coefficient of coupling k with same turns ratio n ($\frac{N_s}{N_p}$). Here we can see that as coupling coefficient increases gain increases.

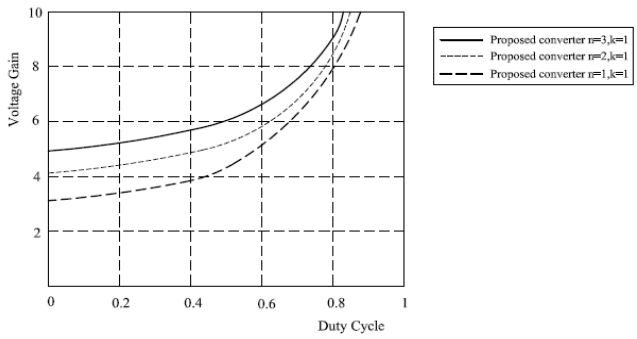

Fig.9. Comparison of voltage gain verses duty cycle for 3 types of converters of [17] , [9] and [1]

In fig.9. we can see that voltage gain of converter [9] and traditional boost converter with same turns ratio n ($\frac{N_s}{N_p}$) and coupling coefficient is much lower than that of proposed converter.

3. System design of the Converter

How to design the magnetizing inductor Lm, the energy transferring capacitor C_1, the charge pump capacitor C_2, the output capacitor C_0, and the output inductor L_0 is shown as follows.

Table. 1 System specifications of proposed

System Parameters	Specifications
Input Voltage (Vi)	12 V
Rated output voltage (V_0)	72 V
Rated output current ($I_{0,rated}$)	0.833 A
Power ($P_{0,rated}$)	60 W
Minimum output current ($I_{0,min}$)	0.1 A
Power ($P_{0,min}$)	7.2 W
Switching frequency (f_s)	100 kHz

4. Design Consideration of Circuit Component

4.1 Calculation of magnetizing inductor

To make sure that Lm always operates in the positive region, the required equation is as follows

$$L_m \geq \frac{V_i D T_s}{\Delta i_{Lm}} = \frac{V_i D T_s}{2 \times I_{Lm,\min}} \quad (20)$$

where $I_{Lm,min}$ is the minimum dc current in Lm. Finally, the value of Lm is set at 148.7 μH.

4.2 Calculation of Output Inductor

From the industrial viewpoint, the output inductor is generally designed to have no negative current when the output current is above 20%–30% of the rated output current [20]. Therefore, in this paper, the boundary between the positive and negative currents is assumed to be at 20% of the rated output current. Hence, the value of L_o can be obtained in (33), shown at the bottom of the page. Eventually, the value of L_o is set at 188 μH.

$$L_0 = \frac{L_0 \Delta t}{\Delta i_{Lm}}$$

$$= \frac{(V_i + V_{C1} + V_{C2} - V_0)(1-D)T_s}{\Delta i_{L0}} \quad (21)$$

4.3 Calculation of Energy-Transferring Capacitor

Assuming the peak-to-peak value of the capacitor voltage during the charge period, i.e., Δv_{C1}, is set to 1% of V_{C1} or less, i.e., Δv_{C1} is smaller than 120 mV, the value of C_1 can be obtained as follows:

$$C_1 \geq \frac{i_{C1} \Delta t}{\Delta V_{C1}}$$

$$= \frac{(I_{i,rated} - I_{0,rated})(1-D)T_s}{(0.001 \times V_{C1})} \quad (22)$$

where $I_{i,rated}$ is the dc input current I_i under rated conditions. Eventually, two 470-μF capacitors with positive terminals connected in series are selected for C_1

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4.4 Calculation of Charge Pump Capacitor

Assuming the variation in capacitor voltage during the discharge period, i.e., Δv_{C2} is set to 0.1% of V_{C2} or less, i.e., Δv_{C2} is smaller than 60 mV, the value of C_2 can be obtained as follows:

$$C_2 \geq \frac{i_{C2}\Delta t}{\Delta V_{C2}} = \frac{I_{Lo,rated}(1-D)T_s}{(0.001 \times V_{C2})} \quad (23)$$

where I_{Lo},rated is the dc current in L_o under rated conditions. Finally, two 47-μF capacitors connected in parallel are chosen for C_2.

4.5 Calculation Output Capacitor

As generally known, the output filter is used to filter out the output current ripple as much as possible. Prior to designing C_o, the output voltage ripple Δv_o is assumed to be smaller than 0.1% of the rated output voltage,i.e., Δv_o is smaller than 72 mV. Therefore, the equivalent series resistance of the output capacitor, i.e., ESR, can be represented by

$$ESR \leq \frac{\Delta V_o}{\Delta i_L} = \frac{0.001 \times V_o}{\Delta i_{Lo}} \quad (24)$$

Eventually, two 220-μF capacitors connected in parallel are selected for C_o

5. Control method applied with design consideration

In order to achieve a constant voltage of 72 V at output stage of the proposed converter we can do two type of control. They are PI control and Fuzzy based control.

5.1 Control of proposed converter based on PI control

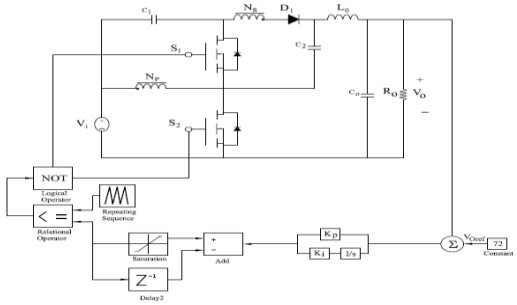

Fig.10. Proposed overall system block diagram based on PI control

Fig.10. shows the overall system block diagram based on PI control. First of all the output voltage is compared with a constant voltage of 72V. Then this error is given to PI controller. Then this signal is compared with a sawtooth signal, the resultant pulse is given to MOSFET S_2 directly and noted and given to MOSFET S_1. There are two steps to tune the parameters of the proportional gain kp and the integral gain ki in the PI controller.

1) Step 1: Start with $k_p = 0$ and $k_i = 0$, and trim kp until a small residual error is received.

2) Step 2: Increase k_i until the system reaches an almost zero final error.

5.2 Control of proposed converter using Fuzzy based control

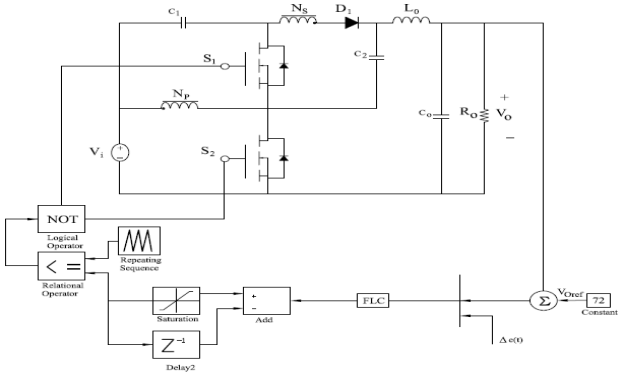

Fig.11. Proposed overall system block diagram using Fuzzy based control

Fig.11. shows the overall system block diagram of proposed converter based on fuzzy control. First of all the output is compared with a constant dc voltage of 72V to produce the error. Here the error and error change are the premises. Then premises are given to fuzzy rule based inference. Here mamdani method is used to infer the rule. Here the crisp value is converted to fuzzified value then it is defuzzified based on the centroid method. Then we will get the error change as crisp value. Then previous error is added to get the error signal. This signal is compared with the sawtooth repeating signal to get the pulses. This pulse is directly given to MOSFET S_2 and noted and given to S_1.

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6. Comparison of fuzzy and PI control based output

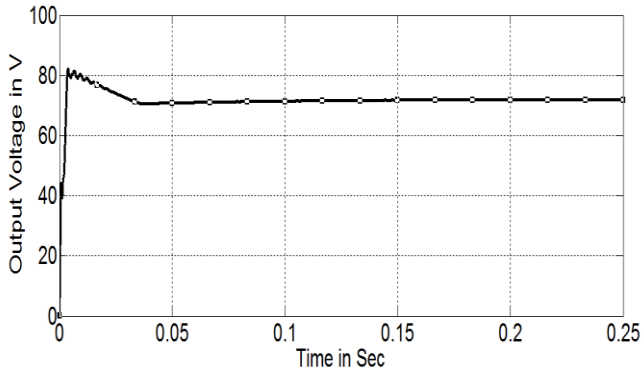

Fig.12. Output voltage based on PI control

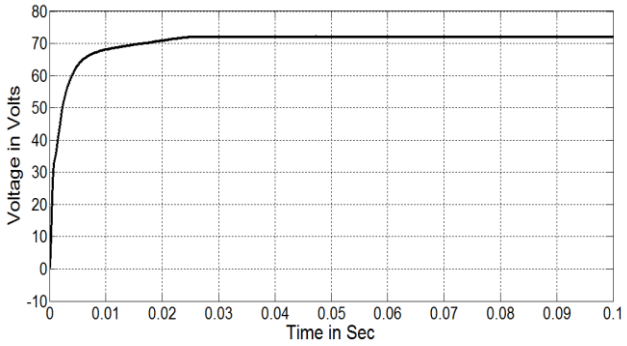

Fig.13. Output voltage based on Fuzzy control

Output of fuzzy based control is free from transients and peak overshoots. More over settling time is less for fuzzy based system compared with PI based control.

7. Experimental set up of the converter

This chapter describes the verification of the proposed system operation with an experimental set up. Hardware set up consists of power circuit, control circuit, gate driving circuit and control circuit power supply.Output voltage from the circuit is given to 4n25 inorder to regulate the voltage.Then this voltage is given to dsPic30f2010 inorder to produce the required gating pulse.This gate pulse is given to FAN7392 which is a gate driver inorder to drive the gate pulse to switch and also provide isolation for power circuit and control circuit.LM317 is used to regulate the voltage.

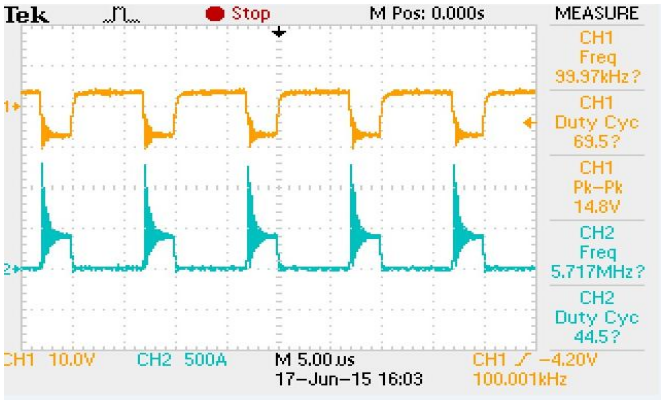

Fig.14. Voltage across switches S_1 and S_2

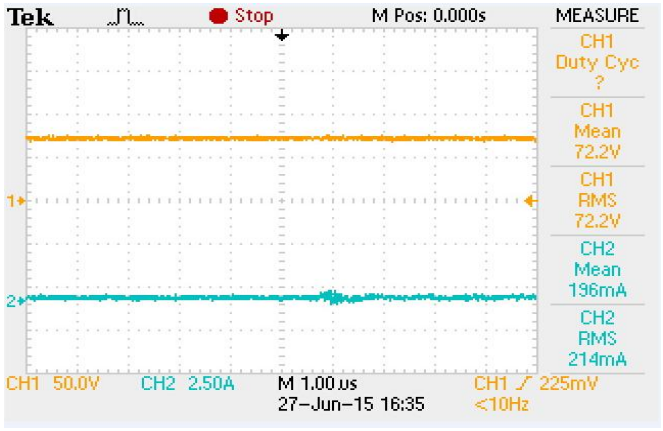

Fig.15. Output Voltage & Current across a load of 400Ω Resistor

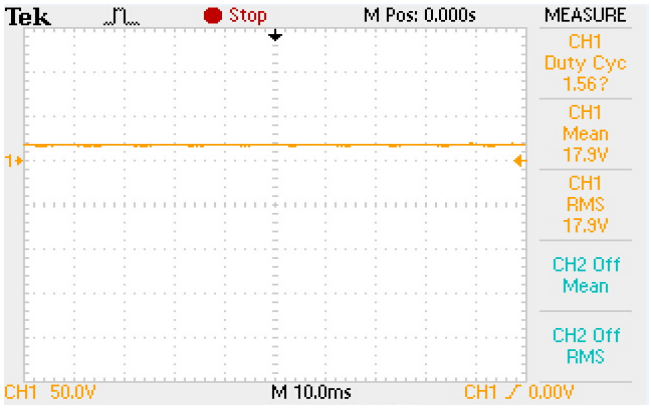

Fig. 16. Voltage across Energy Transferring Capacitor C1

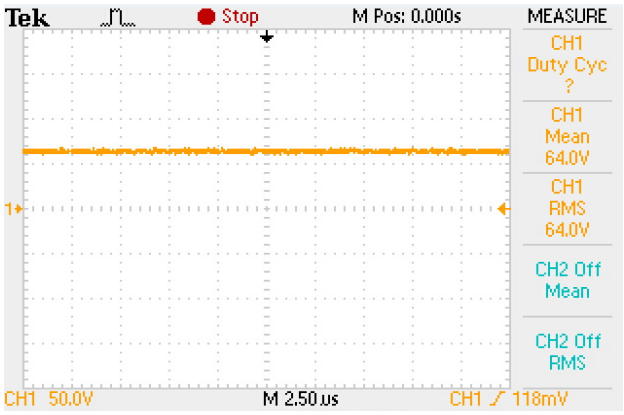

Fig.17. Voltage across Charge Pump Capacitor C2
Hardware results of the proposed closed loop step up DC-DC converter are in agreement with the analysis carried out.

8. Conclusion

A high step-up converter has been presented here. By combining the coupled inductor and the switched capacitor, the corresponding voltage gain is higher than that of the existing step-up converter combining KY and buck-boost converters. Detailed analysis of the single stage converter has been presented. Based on the analysis, designs of various circuit components are presented. Both open loop and closed loop control scheme of the configuration has been explained in detail. Closed loop control is done using two control methods ie; Conventional PI Controller and Fuzzy logic controller. A comparison of the results obtained from the simulation of two control methods is done and can be inferred that Fuzzy based Controller is better than PI Controller. Simulation results show the validation of the proposed topology and its analysis.

The proposed single stage DC-AC inverter has many remarkable features as listed below:

1)Proposed converter has no floating output

2)It has one output inductor; hence, the output current is nonpulsating.

3)The structure of the proposed converter is quite simple and very suitable for industrial applications.

Hardware setup of DC-DC converter is implemented. From 12V DC supply we get 72V DC output voltage from the simulation and hardware. More over the result is valid when load is changed.

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