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HIGH EFFICIENCY BRIDGELESS SEPIC RECTIFIER FOR POWER FACTOR CORRECTION

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Abstract

A step-up bridgeless single phase ac-dc power factor correction (PFC) rectifier based on sepic topology is proposed for high voltage battery charger application. The proposed topology consists of common input stage and parallel output stages. It utilizes one control signal over the whole line cycle. In addition, the proposed converter exhibits low inrush current and low magnetic emissions as classical sepic topology. The bridgeless topology results in lower conduction losses as compared with conventional sepic converter. Simulation results are presented along with the theoretical analysis.

Keywords: Bridgeless rectifier, sepic topology, DCM, low in-rush current and PFC.

1. Introduction

Power supplies with active power factor correction (PFC) techniques are required for wide range of applications for communication, automotive, computer and biomedical industries. All of these applications are required to meet industry standards such as the IEC 61000-3-2. In addition, it is highly recommended to meet new Industry standards such as the 80 PLUS initiative. Many papers have been published in the literature to provide a solution for single-stage power factor correction (PFC) integrated topologies [1-7]. These solutions have been effective to provide cost-effective approach for achieving both the function of high PFC and fast output voltage regulation.

Most of the PFC rectifiers utilize boost converter at their front end. Boost converter provides many advantages such as natural power factor correction capability and simple control. However, low voltage applications such as telecommunication or computer industry an additional converter or an isolation transformer is required to step down the voltage. However, classical boost arrangement has lower efficiency due to significant losses in the diode bridge [1]. In addition, boost converters suffer from high inrush current which increases the cost of safety required disconnection devices between the load and the line voltage. To minimize the losses of the full bridge, many bridgeless PFC rectifiers have been introduced to improve the rectifier power density and/or reduced noise emissions [2]-[5] via soft switching techniques or coupled magnetic topologies. Several non-boost bridgeless rectifiers have been published lately [6]-[10].

In this paper, high efficiency bridgeless sepic topology is proposed. The circuit works in the current DCM, the input current cannot only automatically follow input voltage, and reduced EMI of input current, but also make the switch turn on low-current state, the diode turn off in zero current, which reduce the conduction losses of the switch and the reverse recovery losses of the diode [1]-[7],[10],[11]. In this paper, the working principle of the circuit and derivation of key parameters are presented. And then small-signal mode of the bridgeless SEPIC-PFC circuit is derived, the control mode of the system is established. Finally, the simulation is carried out under the PSIM simulation software. According to the theoretical analysis above, the prototype of the bridgeless SEPIC PFC circuit is made, and the design method and experimental results are given[12]-[20]. Experimental results verify that theoretical analysis and simulation results are correct. The proposed topology's performance is evaluated based on component count, efficiency, total harmonic distortion (THD) and complexity. The proposed topology has an inherent low inrush current. In addition the proposed topology performance is compared with full bridge Cuk converter.

2. Proposed SEPIC PFC converter

Single ended primary-inductor converter (SEPIC) is type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that at its input; the output of the SEPIC is controlled by the duty cycle of the control transistor. The conventional Sepic Rectifier is shown in figure1 [9], [11]. This topology is similar to the bridgeless boost PFC rectifier. Despite the mentioned advantage, in comparison to the conventional SEPIC rectifier, this converter has three extra passive

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elements which contribute to the volume and weight of the converter. Another major problem with this converter is that it doubles the output voltage which considerably increases the size of output filter. To overcome these limitations, a new bridgeless SEPIC PFC is introduced in this paper. This converter has no extra (passive or active) elements in comparison to conventional SEPIC PFC. Also, in this converter, the conduction losses (number of active elements in the current path) are reduced in comparison to the conventional SEPIC PFC. The bridgeless Sepic Rectifier is shown in figure 2. In this converter, the component count is reduced and it shows high efficiency due to the absence of the full-bridge diode. However, in this converter, an input inductor with large inductance should be used in order to reduce the input current ripple.

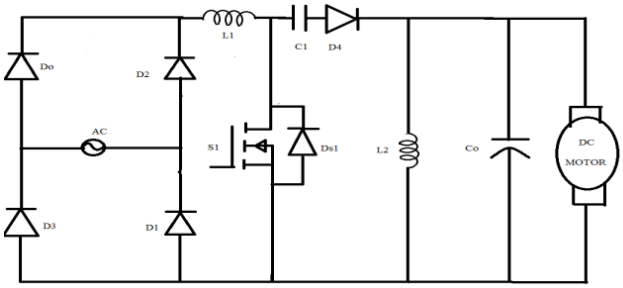

Fig. 1. Conventional Sepic PFC Rectifier

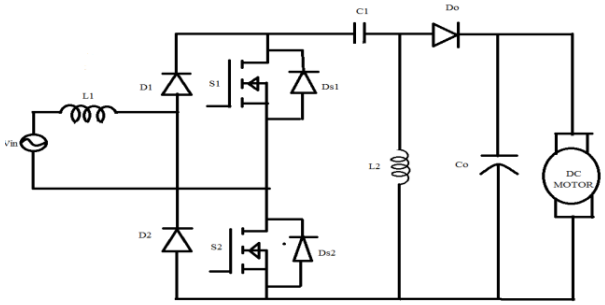

Fig. 2. Bridgeless sepic Converter

The conduction losses on intrinsic body diodes of the switches are caused by using single pulse width modulation (PWM) gate signal. In order to overcome these problems, a bridgeless SEPIC converter is changed in proposed. It is shown in figure 3. An auxiliary circuit, which consists of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor, is utilized to reduce the input current ripple. Coupled inductors are often used to reduce current ripple. The capacitance of the output capacitor Co is assumed sufficiently large enough to consider the output voltage Vo as constant. For a half period of the input voltage, one switch is continuously turned ON and the current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch further and the efficiency can be improved.

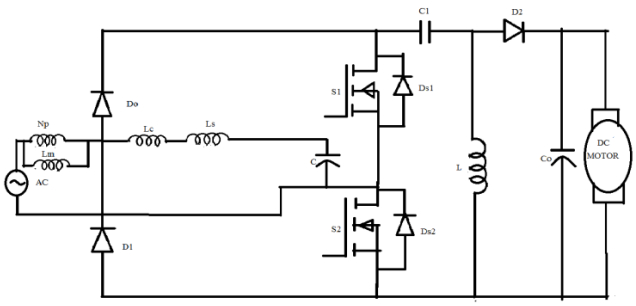

Fig. 3. Proposed Bridgeless sepic Converter

The main difference is that in existing system input ripple current produce more harmonics. And the existing system coupled inductor is not connected. The operation of the proposed converter is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation is analyzed during one switching period in the positive half-line cycle of the input voltage. It is assumed that the converter operates in discontinuous conduction mode (DCM), so the output diode Do is turned OFF before the main switch is turned ON.

3. Analysis of proposed rectifier

The auxiliary circuit includes additional winding Ns of the input inductor L_c, an auxiliary inductor L_s, and a capacitor C. The coupled inductor L_c is modeled as a magnetizing inductance L_m and an ideal transformer which has a turn ratio of 1: n ($n=N_s/N_p$). The leakage inductance of the coupled inductor L_c is included in the auxiliary inductor L_s. The other components C_1, L_1, D_o, and C_o are similar to those of the conventional SEPIC PFC converter.

Diodes D_1 and D_2 are the input rectifiers and operate like a conventional SEPIC PFC converter. D_{s1} and D_{s2} are the intrinsic body diodes of the switches S_1 and S_2. The switches S_1 and S_2 are operated with the proposed gate signals.

Mode 1 [t_0, t_1]:

At t_0, the switch S_1 is turned ON and the switch S_2 is still conducting. Since the voltage v_p across L_m is V_{in} , the magnetizing current i_m increases from its minimum value I_{m2} linearly with a slope of V_{in}/L_m. It is shown in figure 4.

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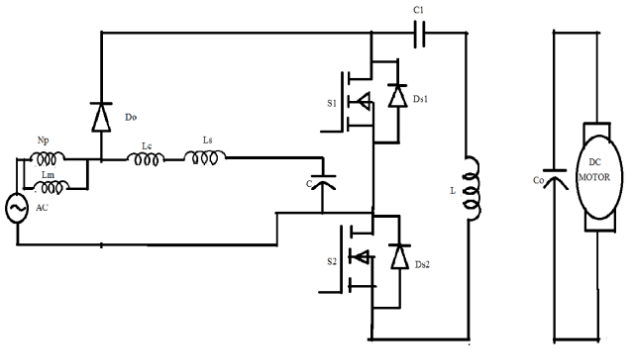

Fig. 4. Mode 1 operation

Mode 2 [t_1, t_2]:

At t_1, the switch S_1 is turned OFF and the switch S_2 is still conducting. Since the voltage v_p across L_m is $-V_o$, the magnetizing current i_m decreases from its maximum value Im1 linearly with a slope of $-V_o / L_m$. It is shown in figure 5.

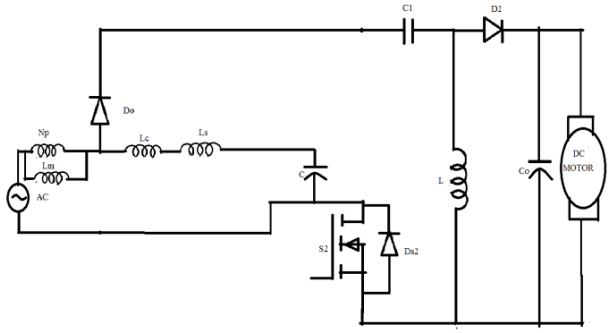

Fig . 5. Mode 2 operation

Mode 3 [t_2, t_0]:

At t_2 , the current i_{Do} becomes zero, and the diode D_o is turned OFF. Since $i_{in} = i_m - n_{is} = -i_s - i_{L1}$ in this mode, the input current i_{in} is the sum of freewheeling Currents I_{s2} and I_{L2}. It is shown in figure 6.

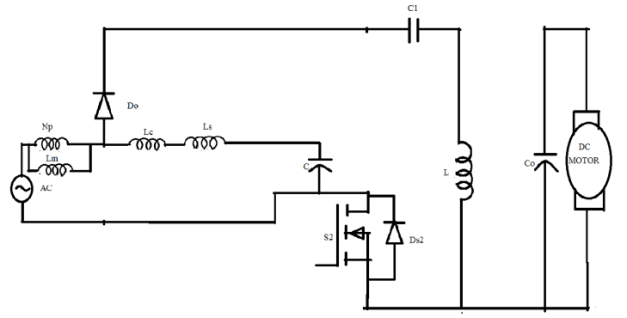

Fig. 6. Mode 3 operation

4. Simulation result

Sim Power Systems libraries contain models of typical power equipment such as transformers, machines, lines and transformers. The capabilities of SimPowerSystems software for modeling a typical electrical system are illustrated demonstration files. And for users who want to refresh their knowledge of power system theory, there are also self-learning case studies. The Sim Power Systems main library, powerlib, organizes its blocks into libraries according to their behavior. To open this library, type powerlib in the MATLAB Command Window. The power lib library window displays the block library icons and names. Double-click a library icon to open the library and access the blocks. The main powerlib library window also contains the Powergui block that opens a graphical user interface for the steady-state analysis of electrical circuits. The simulation circuit diagram is shown in figure 7.

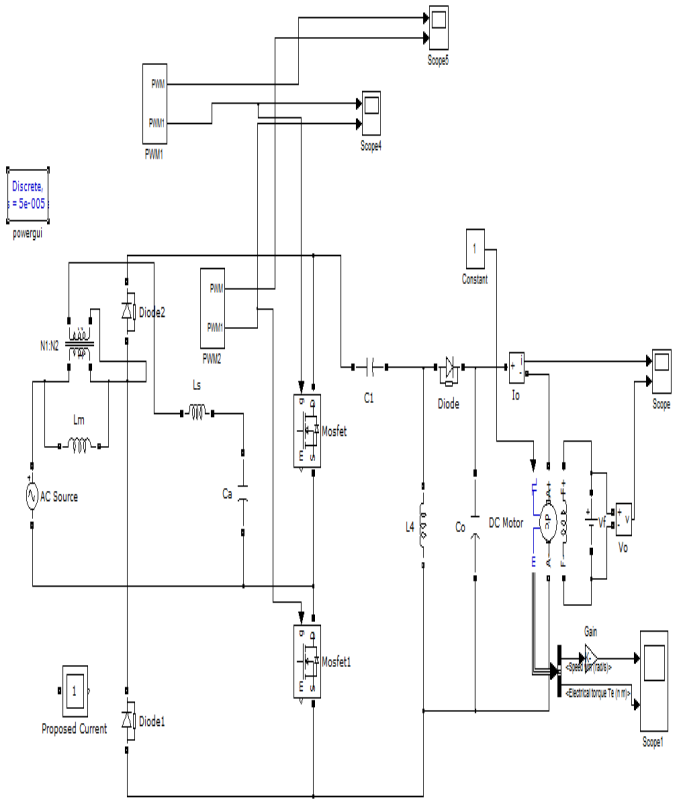

Fig.7. simulation circuit diagram

The carrier PWM output waveform is shown infig.8.

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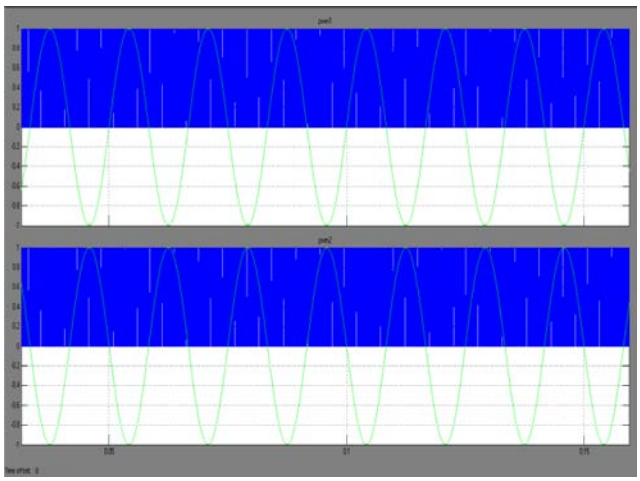

Fig.8. carrier pwm output waveform

The PWM pulse output waveform is shown in figure 9.

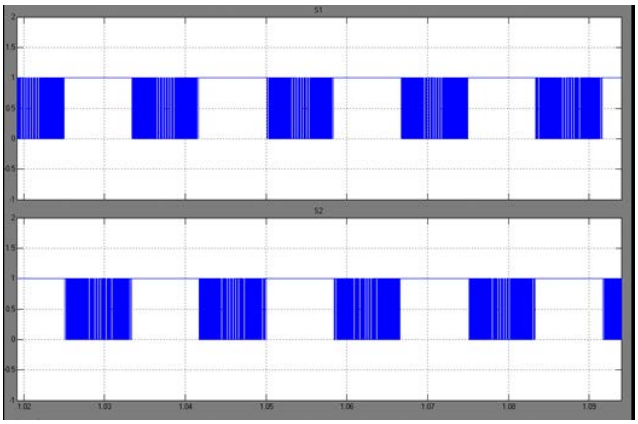

Fig .9.pwm pulse output

The current ripple waveform is shown in figure 10.

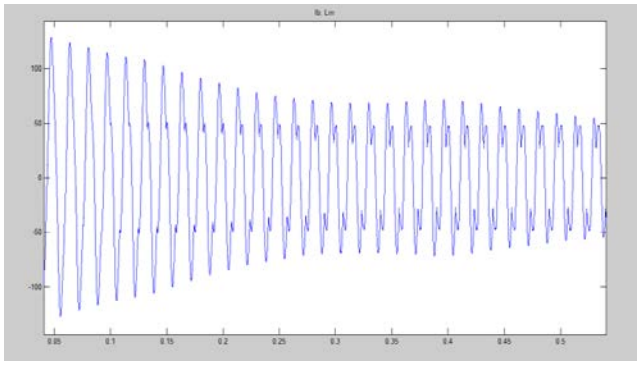

Fig .10.current ripple

The output current and output voltage waveform of dc motor is shown in fig 11.

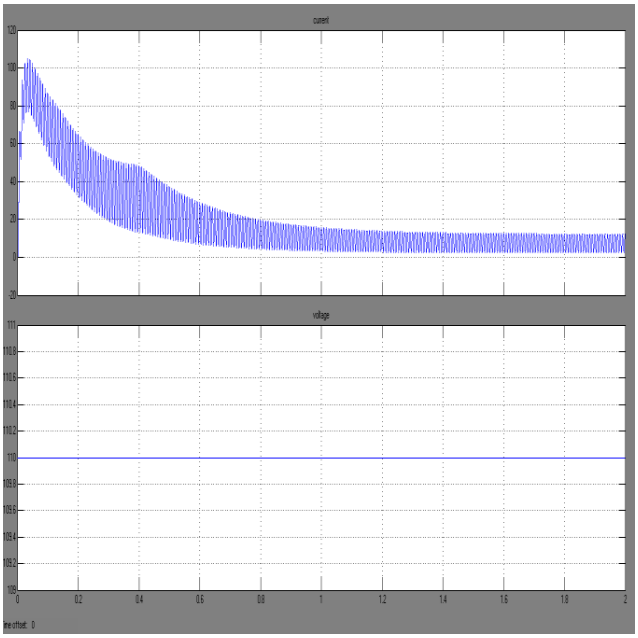

Fig.11 output current and voltage waveform of dc motor

The speed and torque waveform of dc motor is shown in figure 12.

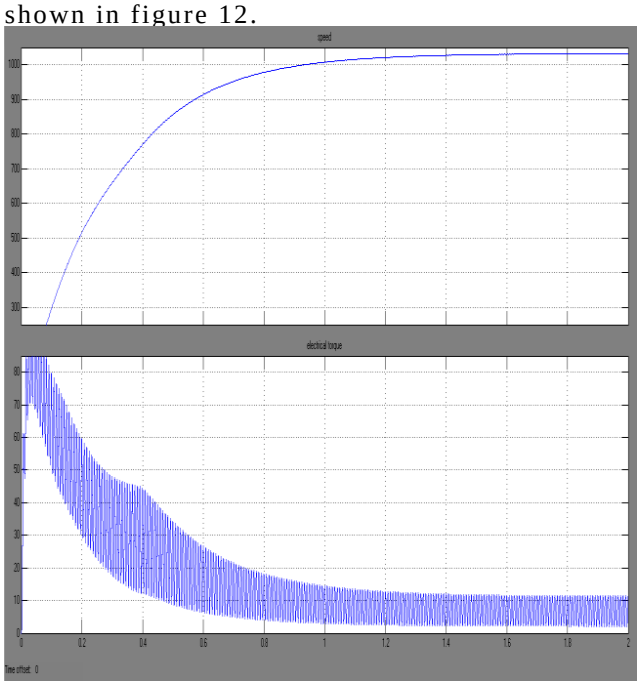

Fig.12 speed and torque waveform of dc motor

The harmonic of sepic converter with power factor correction fed dc motor is shown in fig 13.

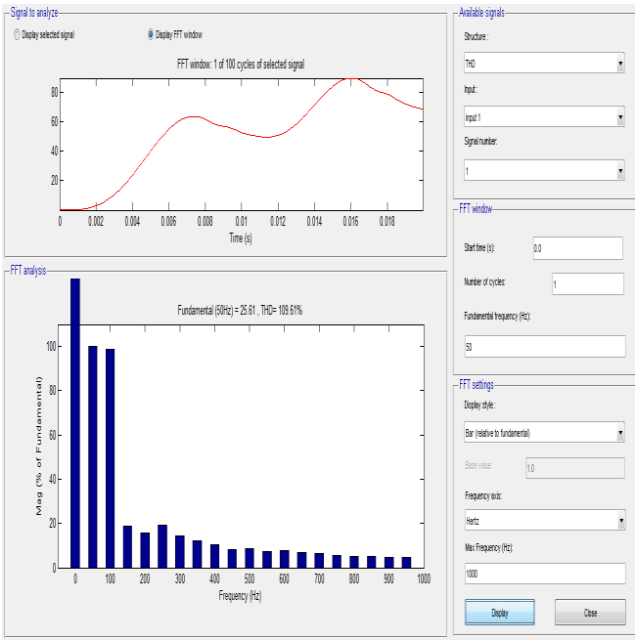

Fig.13 Harmonic of sepic converter with power factor correction

5. Conclusion

A bridgeless SEPIC converter with ripple-free input current has been proposed. In order to improve the efficiency, the input full-bridge diode is eliminated. The input current ripple of the proposed converter is significantly reduced by utilizing an auxiliary circuit consisting of an additional winding of the input inductor, an auxiliary small inductor, and a capacitor. The theoretical analysis, simulation results, and experimental results were provided.

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