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Design of Low Power 8-bit Carry Select Adder

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Abstract

In this project an efficient high-sped 8-bit carry select adder. The adder is designed and implemented using CMOS process technology. The proposed adder provides a good compromise between cost and performance in carry propagation adder design. It decreases the computational time compared to ripple carry adder and thus increases the speed. The carry select adder consists of 4-bit ripple carry adders and an array of 2:1 multiplexers. The carry is selected through the multiplexer. The layout of the design is efficiently optimized in terms of area using CMOS technology micron rules. The performance of the adder and its blocks is analysed in terms of different performance parameters. Various foundry technologies are implemented for the 8-bit CSA and comparison is done among. The lowest power dissipation is proposed among these.

Keywords: *CMOS, Carry Select, Power Dissipation*

1. Introduction

Addition is the heart of computer arithmetic and the arithmetic unit is often the work house of a computational circuit. There are many ways to design adder. The ripple carry adder (RCA) provides the most compact design but takes longer computing time. If there is N-bit RCA, the delay is linearly proportional to N. Thus for large values of N the RCA gives highest delay of all the adders. The carry look ahead adder (CLA) gives fast results but consumes large area. If there is N-bit adder, CLA is fast for N≤4, but for large values of N its delay increases more than other adders. The problem of the ripple-carry adder is that each adder has to wait for the arrival of its carry-input signal before the actual addition can start. The basic idea of the carry select adder [1] is to use blocks of two ripple carry adders, one of which is fed with a constant 0 carry-in while the other is fed with a constant 1 carry-in. Thus, both blocks can calculate in parallel. When the actual carry-in signal for the block arrives, multiplexers are used to select the correct one of both precalculated partial sums. Also, the resulting carry-out is selected and propagated to the next carry select block. Hence, the time for the implementation of carry select adder is expressed in equation 1, where

$t_{RCAcarry}$ is the delay for the carryout of a full adder
t_{RCAsum} is the delay for the sum of a full adder
Propagation Delay ($t_{RCAprop}$) = (N-1) × ($t_{RCAcarry}$ + t_{RCAsum}) (1) From equation 1, we can see that the delay is proportional to the length of the adder. An example of a worst case propagation delay input pattern for a 4 bit ripple-carry adder is where the input operands change from 1111 and 0000 to 1111 and 0001, resulting in a sum changing from 01111 to 10000.

The proposed carry select adder is implemented using DSCH EDA tool we propose a design and implementation of 8-bit carry select adder. The paper is organized as follows: in section 2, basics of carry select adder is presented. Subsequently, in section 3, the implementation of the adder is presented. In section 4, the schematic and layout of the adder is presented. In section 5, the simulation results are given and discussed. The evaluation of performance parameters for the proposed design is carried out. Finally a conclusion will be made in the last section.

Carry select adders

Carry select adders use multiple narrow adders to create fast wide adders used in many data processing processors to perform fast arithmetic operations. Consider the addition of two n-bit numbers with a=a(n-1)……..a(0) and b=b(n-1)……..b(0). At the bit level, the adder delay increases from the least

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significant 0th position upward, with the (n-1)th requiring the most complex logic. A carry select adder breaks the addition problem into smaller groups. For example, we can split the n-bit problem into two (n/2)-bit-selections, then give special attention to the higher order group that adds the word segments a(n-1)…….a(n/2) and b(n-1)…….b(n/2). The carry delay will then center around the carry-out bit c(n/2) produced by the sum of lower order word segments a(n/2-1)…….a(0) and b(n/2-1)…..…b(0). We know that there are only two possibilities for the carry bit, c(n/2)=0 or c(n/2)=1.A carry-select adder provides two separate adders for the upper words, one for each possibility. A multiplexer is then used to select the valid result.

2. IMPLEMENTATION OF 8-BIT CSA

The 8-bit carry select adder [2] is implemented as shown in Figure 1.The adder is split into two 4-bit groups. The lower order bits a3 a2 a1 a0 and b3 b2 b1 b0 are fed into the 4-bit adder L to produce the sum bits s3 s2 s1 s0 and a carry-out bit c4. The higher order bits a7 a6 a5 a4 and b7 b6 b5 b4 are used as inputs to two 4-bit adders.

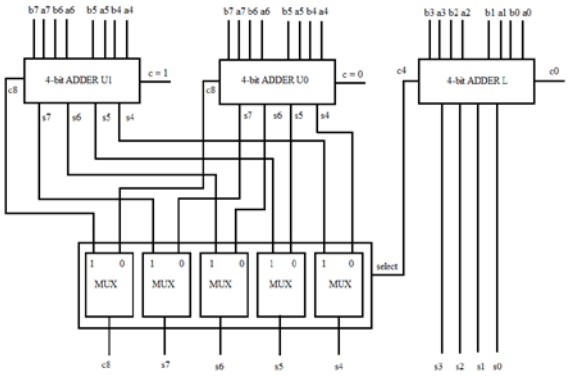
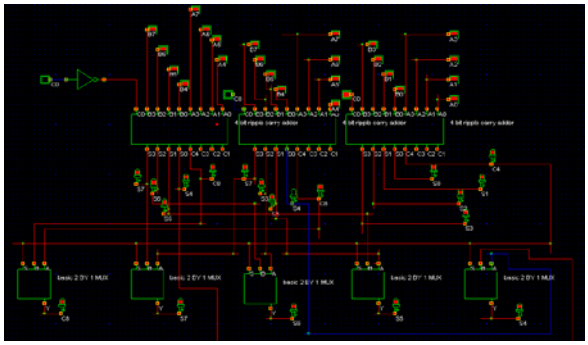


Fig1. *8-bit Carry Select Adder*



Adder U0 calculates the sum with a carry-in of c=0, while adder U1 calculates with a carry-in of c =1. Both sets of results are used as inputs to an array of 2:1 multiplexers. The carry bit from the c4 of adder L is used as the MUX select signal. If c4 = 0, then the results of U0 are sent to the output, while a value of c4 =1 selects the results of U1 for s7 s6 s5 s4. The carry-out bit c8 is also selected by the MUX array.

2.1 Implementation of 4-Bit Adder

The 4-bit adder block used in CSA is ripple carry adder. In ripple carry adder each carry bit from a full adder "ripples" to the next full adder [3]. The simple implementation of 4-bit ripple carry adder is shown below in Figure 2. C0 is the input carry, x3 x2 x1 x0 and y3 y2 y1 y0 represents two 4-bit input binary numbers.C4 is the output carry and s3 s2 s1 s0 is the sum output.

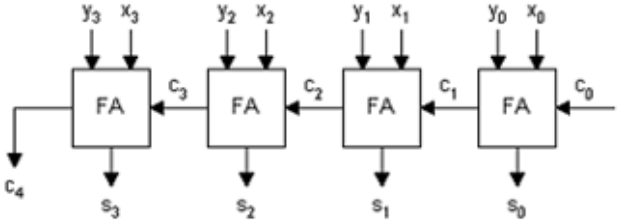
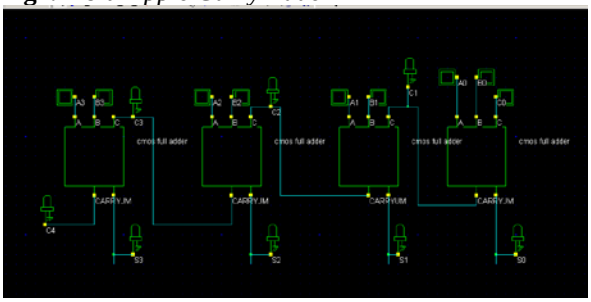


Fig2. *4-bit Ripple Carry Adder*



The ripple carry adder is designed using a full adder cell with 18-transisitors based on transmission gate logic [4]. The full adder is constructed using an XOR gate and two 2:1 multiplexers as shown in Figure 3.The SUM (A xor B xor Cin) is formed by a multiplexer controlled by A xor B (and complement). Examining the adder truth table reveals that when A xor B is true, COUT=C and SUM=complement of C. When A xor B is false, COUT=A (or B) and SUM=C.

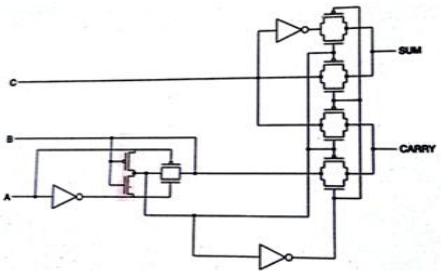
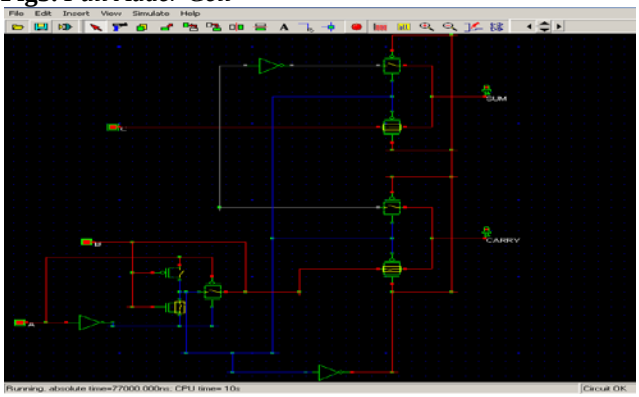


Fig3. *Full Adder Cell*



2.2 **Implementation of 2:1 Multiplexer**

In this design of multiplexer, two transmission gates are used as shown in Figure 4. The transmission gates select input A or B on the basis of the value of the control signal S. When S=0, Y=A and when S=1, Y=B.

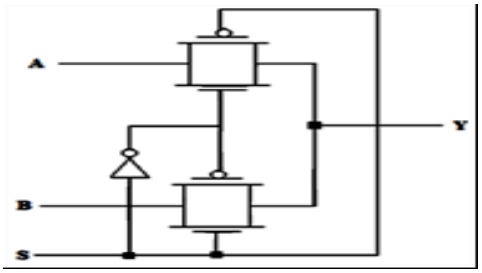
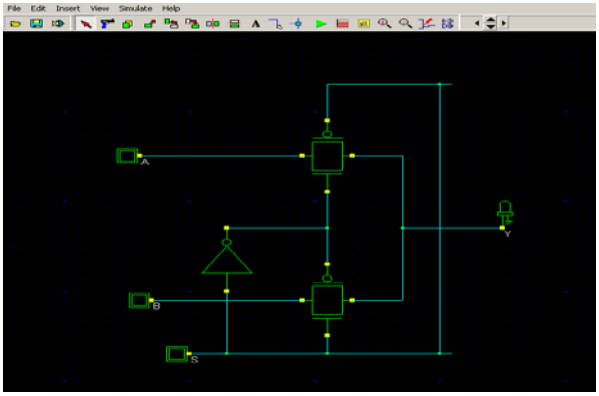


Fig4. *2:1 Multiplexer*



3. Tables, Figures and Equations

3.1 Tables and Figures

Table 1: 8-bit CSA Power Consumption

Circuit	***Transistor Count***	Power Consumption in mW
8-bit CSA	246	10.412 for 180nm
8-bit CSA	246	2.832 for 12nm
8-bit CSA	246	1.408 for 90 nm

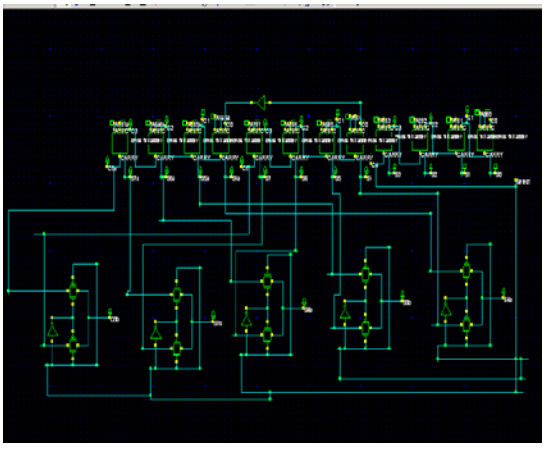


Fig. 5. Proposed 8-bit CSA.

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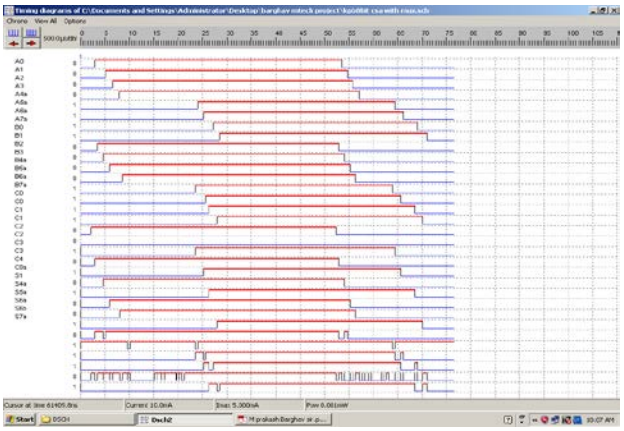

Fig. 6. Simulation of 8-bit CSA.

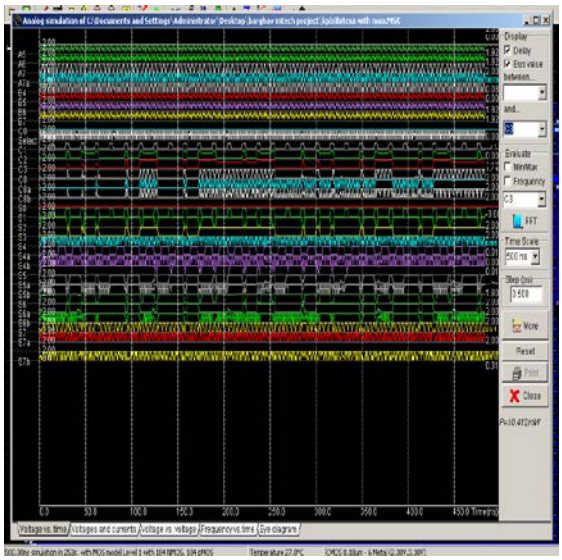

Fig. 8. Analog Simulation of 8-bit CSA using 180nm Technology

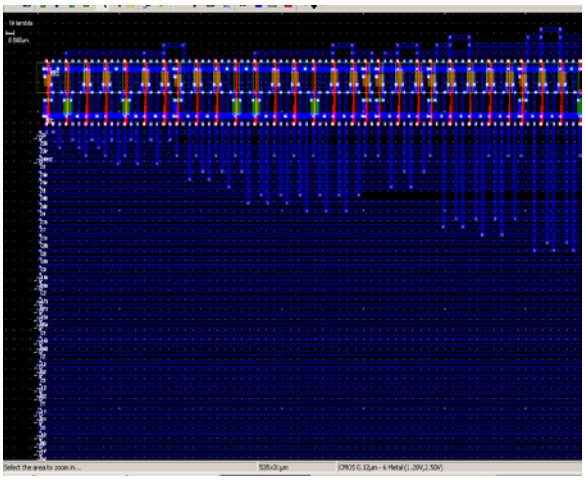

Fig. 7. Layout of 8-bit CSA.

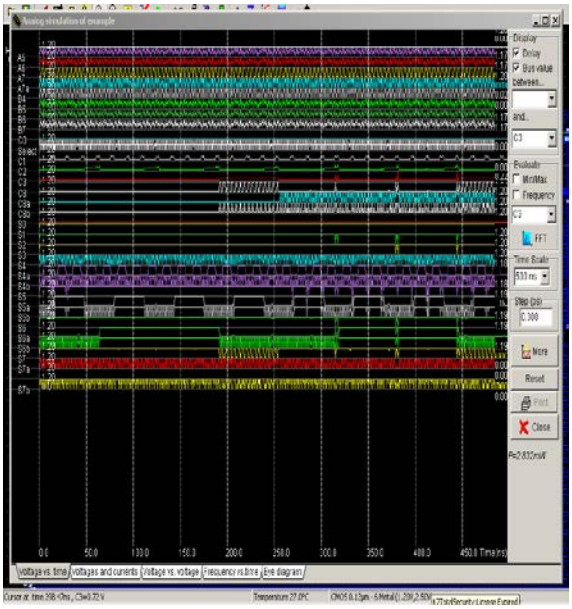

Fig 9. Analog Simulation of 8-bit CSA using 120nm Technology

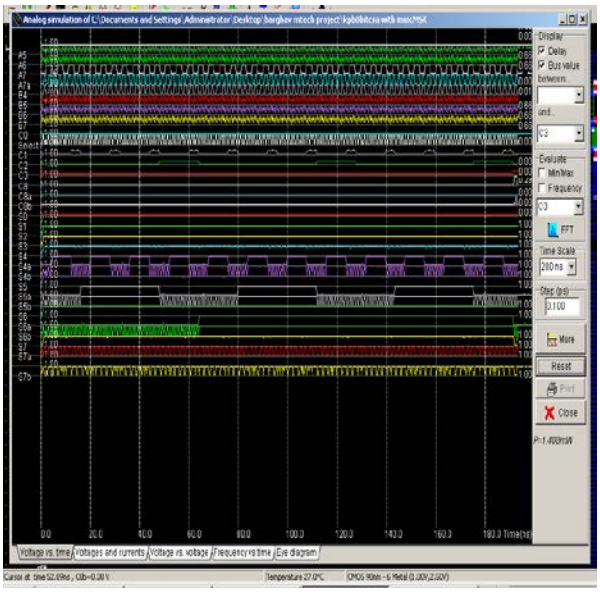

Fig.10. Analog Simulation of 8-bit CSA

using 90nm Technology

3.2 Equations

Power = Energy/transition * transition rate

$$P = C_L * Vdd^2 * f \quad (1)$$

Delay= $$t_{pLH} = \frac{C_L V_{DD}}{k_n (V_{DD} - V_{Tn})^2} \quad (2)$$

Power Reduction is

$$P_{ref} = C_{ref} V_{DD}^2 f_{ref} \quad (3)$$

4. Conclusions

In this paper a novel 8-bit carry select adder is presented which overcomes certain drawbacks of ripple carry adder. The adder is designed using 180nm,120nm,90nm CMOS process technology. In ripple carry adder each block has to wait for the carry output of the previous block and thus propagation delay increases. The carry select adder efficiently overcomes this drawback by reducing the computational time and thus increases the speed. The performance of the design is analyzed in terms of transistor count, propagation delay and power consumption. The layout of the design is efficiently optimized based on 180nm, 120nm,90nm micron rules. From above Table 1: 8-bit CSA Power Consumption, 90 nm technology is having lowest power among the three technologies. In future still a low power consumption technology can be obtained without degradation of the functionality of the circuit

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References

[1] John P. Uyemura, "Introduction to VLSI circuits and systems".

[2] Sarabdeep Singh and Dilip Kumar, "Design of area and power efficient modified carry select adder", International Journal of Computer Applications (0975 – 8887) Volume 33– No.3, November 2011.

[3] Dan Wang, Maofeng Yang, Wu Cheng XUguang Guan, Zhangming Zhu, Yintang Yang " Novel low power full adder cells in 180nm CMOS technology", 4th IEEE conference on Industrial Electronics and Applications, pp. 430-433,2009.

[4] Neil H. E. Weste, Kamran Eshranghian, " Principles of CMOS VLSI design", A systems perspective, 2nd edition.

[5] Cadence Analog and Mixed signal labs, revision 1.0, IC613, Assura 32, incisive unified simulator 82, Cadence design systems, Bangalore.

[6] Kuldeep Rawat, Tarek Darwish and Magdy Bayoumi, "A low power and reduced area carry select adder", 45th Midwest Symposium on Circuits and Systems, vol.1, pp. 467-470, March 2002.

[7] O. J. Bedrij, "Carry-select adder", IRE transactions on Electronics Computers, vol.EC-11, pp. 340-346, June1962.

[8] I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin and Chien-Chang Peng, "An area-efficient carry select adder design by sharing the common boolean logic term" Proceedings of the International Multiconference of Engineers and Computer Scientists 2012 Vol. II, IMECS 2012, March 14-16 2012, Hong Kong.

[9] Behnam Amelifard, Farzan Fallah, Massoud Pedram, "Closing the gap between carry select Adder and ripple carry adder: A new class of low-power high-performance adders".

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