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Fast Protection of Strong Power System With Fault Current Limiters and PLL - Aided Fault Detection

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***Abstract*— In this paper we used to discriminate faults from switching transient ,fast fault detection and fast fault clearing before the first peak of fault current are required in this system a phase locked loop system is to be taken for the discrimination computer simulations have been performed in this system phase locked loop output is completely different for a fault compared to the switching transient**

Keyword :fault current limiters ,superconducting fault current limiters,fault current diverters,power system protection,phase locked loop,

I. INTRODUCTION

The introduction of new generating facilities by independent power producers and increasing load demand can result in fault current over duty on existing transmission system protective equipment. Conventional solutions to fault current over duty such as major substation upgrades, splitting existing substations buses or multiple circuit breakers upgrades could be very expensive and require undesirable extended outages and result in lower power system reliability. Due to the difficulty in power network reinforcement and the interconnection of more distributed generations, fault current level has become a serious problem in transmission and distribution system operations. The utilization of fault current limiters (FCLs) in power system provides an effective way to suppress fault currents.

Large-scale power systems are required to meet the increasing demand for electricity. For such systems, the fault current that occurs for short-circuit faults is higher and existing breakers may not be suitable for current interruption. In addition, the large voltage generated by electromagnetic induction can lead to communication failures. To address these issues, power system reorganization and circuit breaker upgrades can be considered. Fault condition may result in an electric power transmission system from events such as lightning striking a power line, or downed trees or utility poles shorting the power lines to ground .The fault creates a Surge of current through the electric power system that can cause serious damage to grid equipment. Switchgears ,such as circuit breakers, are deployed within transmission substations to protect substation equipment

II. FAULT CURRENT LIMITERS

A fault current limiter (FCL) limits the amount of current flowing through the system and allows for the continual, uninterrupted operation of the electrical system, similar to the way surge protectors limit damaging currents to household devices. Currently, two broad categories of FCL technologies exist: high-temperature superconducting and solid-sta. need for FCLs is driven by rising system fault current levels a energy demand increases and more distributed generation and clean energy sources, such as wind and solar, are added to an already overburdened system. Currently, explosive fault-limiting fuses are utilized to limit fault current, but they require a service call to replace the fuse after it blows and they are only available for voltages below 35 kV. Series reactors are also used but they have constant high reactive losses, are bulky, and contribute to grid voltage drops. FCLs overcome Additionally, rising fault current levels increase the need for larger and often costly high impedance transformers. However, in contrast to these transformers, FCLs operate with little to no impedance during normal operation which allows for a more stable system. Fault Current Limiter (FCL) is applied to limit very high current in high speed when faults occur

III . SUPER CONDUCTING FAULT CURRENT LIMITERS

Superconducting Fault Current Limiter (SFCL) is innovative electric equipment which has the capability to reduce fault current level within the first cycle of fault current The application of the fault current limiter (FCL) would not only decrease the stress on network devices, but also can offer a connection to improve the reliability of the power system. There are various types of FCLs, which are made of different

superconducting materials and have different designs. They are categorized into three broad types: the resistive type, the inductive type and bridge type SFCL. We discussed the operating characteristics of SFCL introduced into a simplified power transmission model system

Applications of SFCL in power system

1) Limit the fault current
2) Secure interconnector to the network
3) Reduces the voltage sag at distribution system

IV. PHASE LOCKED LOOP

A phase-locked loop is a feedback system combining a voltage controlled oscillator (VCO) and a phase comparator so connected that the oscillator maintains a constant phase angle relative to a reference signal. Phase-locked loops can be used, for example, to generate stable output high frequency signals from a fixed low-frequency signal.

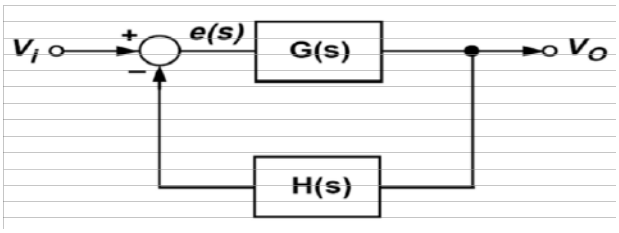

Fig 1 Standard negative Feedback control system model

A PLL is a circuit that is used to synchronize an input signal with a reference signal (an output signal that is generated by the PLL) with respect to phase and frequency. The function of the PLL can be explained from the block diagram of a simple PLL as shown in the FIG 1 The input signal $u_1(t)$is compared with the reference signal $u_2(t)$ in the phase detector (PD). The output of the phase detector is zero as long as the input signal and the

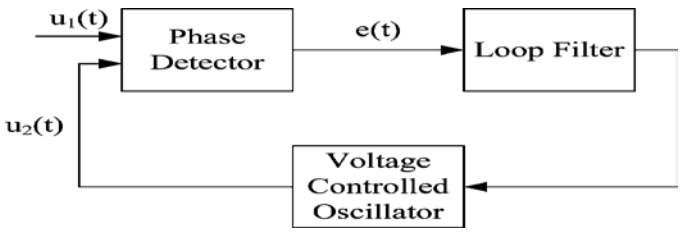

Fig Block diagram of PLL

Output signal is equal in phase and frequency. If the phase or frequency of the input signal changes, the output of the phase detector will deviate from zero. The error signal is passed through a low-pass filter (LF) and then to a voltage-controlled oscillator (VCO), which generates a reference signal (the output signal). If the error signal deviates from zero, the VCO will adjust the frequency of the reference signal so that the phase error becomes zero and the two signals are in phase. When the input signal is in phase with the reference signal, the PLL is in its locked state; hence the named phase locked loop

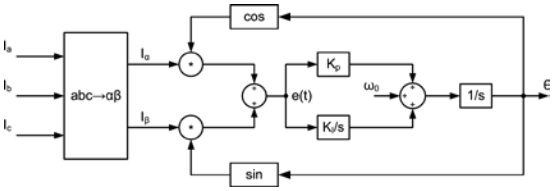

Fig 3.implementation of PLL

A vector implementation, as shown in Fig. 2, of a PLL is described in this paragraph. Compared to the block diagram of Fig. 1, the error signal e (t) corresponds to the output of the PD, whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage-controlled oscillator (VCO). The inputs to the PLL are the three phase-currents (I_a, I_b, i_c) which are first transformed to αβ quantities using (I_α, I_β) Clarke's transformation. Then the αβ quantities are projected onto a reference frame. Depending on the proximity of the αβ quantities to the reference frame, an error signal is formed.

Equations

$$i_a = i.\sin(\omega t)$$

$$i_b = i.\sin\left(\omega t - 2*\frac{\pi}{3}\right)$$

$$i_c = i.sin\left(\omega t + 2*\frac{\pi}{3}\right)$$

Then the Clarke's component $i_\propto$ and i_β equate to

$$i_\propto = \frac{(2.i_{a-}(i_b + i_c))}{3} = Isin(\omega t)$$

$$i_\beta = \frac{(i_{b-i_c})}{\sqrt{3}} = -I\cos(\omega t)$$

Now with reference to fig 2 the error signal is given by

$$e(t) = i_\propto.\cos(\theta) + i_\beta.\sin(\theta) = Isin(\omega t - \theta)$$

Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient Occurs in the system, the error signal will deviate from zero.

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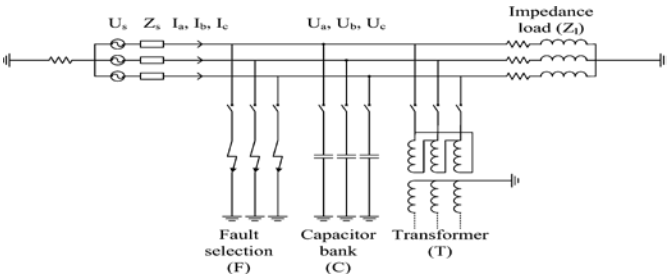

Fig 4 PSCAD/EMTDC SYSTEM

The test system, as shown in Fig. 4, consists of an infinite source, an impedance load, a shunt capacitor (with an associated circuit breaker), a transformer (with an associated CB), and a fault selection arrangement. The data of the system are summarized as follows.

• The infinite source is modeled with a voltage source that is connected in series with an impedance. The supply voltage of the source has been chosen as $U_h = 12$ kV. The series impedance has been chosen so that the power system will have a short-circuit power of approximately $S_k = 831$ MVA (R=12.2mΩ L= 0.55 mH). The supply frequency of the voltage source is selected to 50 Hz. A short-circuit power of 831MVA will give a short-circuit current of approximately$I_k = 40$ kA in this system the shunt capacitor is modeled as a capacitance c=90.19μF.the reactive power supply of shunt capacitor gives 4.08 MVA_r at nominal voltage

VI .FAULT CURRENT DIVERTERS

A fault current diverter for use with high voltage electrical equipment is operative to divert fault current to ground by establishing a non-arcing low impedance current path to ground. The diverter includes a switching device having a moving contact which, in response to the triggering of a chemical propellant charge, is rapidly driven so as to pierce solid insulation and make contact with a high voltage conductor or terminal thereby to establish the non-arcing low impedance path .This invention relates to high speed fault current diverters for use in association with high voltage electrical equipment. The invention is especially applicable to a device for protecting against hazardous failures of underground distribution equipment .A self-contained high speed fault current diverter apparatus for use with high voltage electrical equipment including a high voltage terminal, mounted on a bushing well comprising:

One common feature of the described fault–current limiters and current diverters is that they must be able to operate within a few milliseconds after fault inception. The fault current must be limited before the first peak of the fault current. Taking into account that some of the fault-current limiters described before contain mechanical systems that require a certain time to operate.

VII.POWER SYSTEM PROTECTION

Power system protection is important issue, in power system protection the faults are cleared automatically in fast and reliable manner so it is safe operation In electrical network, there are various faults, such as lightning, short circuits, grounding etc., which occurs large fault current. If these large currents are not properly controlled for power system security, there happens unexpected condition like fire, equipment and facility damage, and even blackout. Therefore, Circuit Breakers are installed and have the duty to cut off fault current, however, it takes minimum breaking time to cut out and sometimes fails to break Fault Current Limiter (FCL) is applied to limit very high current in high speed when faults occur. A protective relay is an IED designed to sense power system disturbances and automatically perform control actions on the I&C system and the power system to protect personnel and equipment. Protective relays are categorized depending up on the component which are protect: generators, transmission lines, transformers, loads

PROTECTION AGAINST EXTERNAL VOLTAGES

Flash on overhead lines caused by lighting surges seldom cause permanent damage provided the line is equipped with high speed protection so that the duration of the power frequency fault current in the fault frequency is limited

(a) Reducing the magnitude the first steepness or frequency of Occurrence of surges at the point where they are initiated by providing shielding earth wires on overhead lines

(b)limiting the magnitude of surges at points where they could be most harmful this requires protection of plant at substation and whilst the inherent protective features of system may be utilized ,it is still usually necessary to limit the magnitude of surges at substations by limiting devices for example protective gas or surge diverters

VIII. RESULTS

In this project the results are taken from the

1 .FAULTS

2 .TRANSFORMER ENERGIZATION

3. CAPACITOR ENERGISATION

1 .FAULTS: in this faults case phase voltages and currents due to a three- phase fault and the error signal due to a three-phase fault (in per unit) is taken and phase voltages and currents due to a phase to phase fault as well as error signal due to a phase to phase fault (per unit is taken) are to be simulated from fig 3 and fig 4 and then results are to be taken

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2 .TRANSFORMER ENERGIZATION: phase voltage and currents due to transformer energization and error signal due to transformer energisation are to be simulated from the fig 3 and fig 4 and results are to be taken

3. CAPACITOR ENERGIZATION: phase voltages and currents due to capacitor energisation are taken and error signal due to capacitor energisation are to be taken and results are to be taken

A. SIMULATED EVENTS :

A large selection of shunt faults, capacitor energizations and Transformer energizations have been simulated. The faults were simulated as three-phase faults and phase-to-phase faults with low impedance. This selection was made because these types of faults are dimensioning for fault-current-limiting applications. Many distribution systems are earthed through an impedance, which limits the magnitude of fault currents due to single-phase earth faults. The capacitor and transformer energizations have been simulated by closing the associated CB.

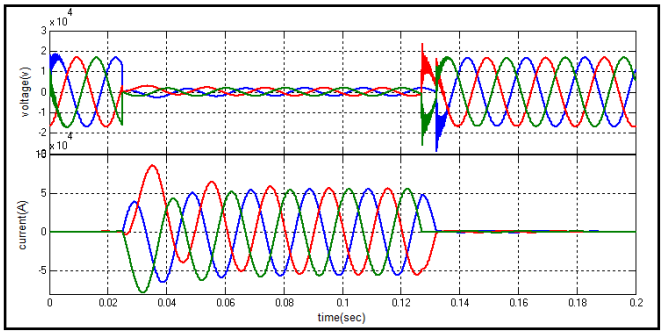

Fig 5 phase voltages and currents due to three phase fault

This section contains plots of signals caused by shunt faults in power system both three phase and phase to phase faults have been analyzed typical phase voltages and currents due to three phase plot are plotted

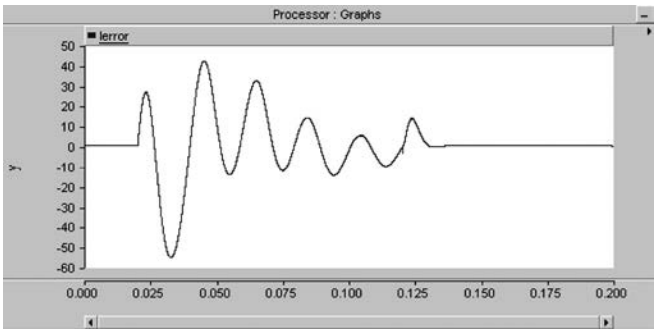

Fig 6 Error signal due to three phase fault
The error signal of the PLL for this fault is plotted in fig 6 in this fig error signal deviates largely from zero shortly after the fault.

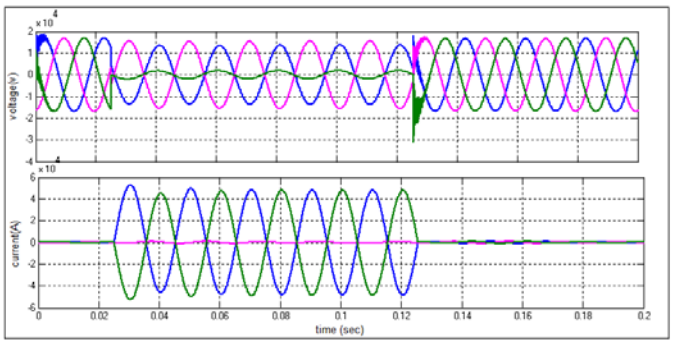

Fig 7 phase voltages and currents due to phase to phase fault

In fig 7 phase voltages and current due to phase to phase fault is plotted in this x axis is taken as the time in(sec) and y axis as voltage and current has been taken.

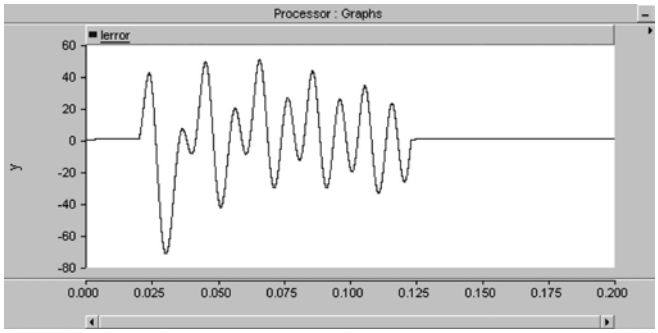

Fig 8 error signal due to phase to phase fault
In fig 8 error signal due to phase to phase fault has been taken

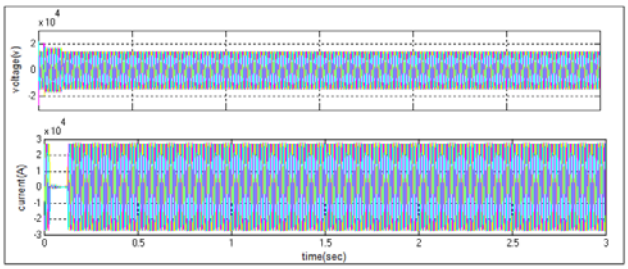

Fig 9. Phase voltages and currents due to capacitor energization
In this capacitor energization have been simulated by closing all the associated circuit breaker all events have been simulated to occur at the various times with respect to the phase angle of supply voltage

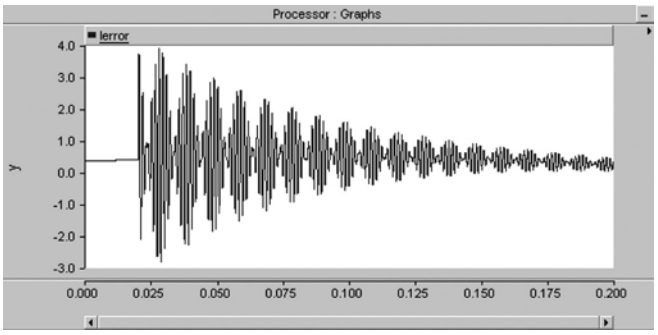

Fig 10.error signal due to capacitor energization

The error signal deviates from zero shortly after the event has been occurred but returns to the steady state when the PLL has been adapted to the new conditions the error signal was never above 5 P.U

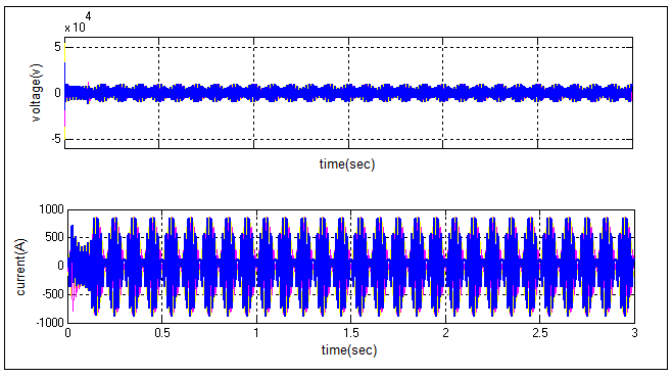

Fig 11. Phase voltages and currents due to transformer energization

In the transformer energization have been simulated by closing all the associated circuit breaker in this section ,plots of signals caused by the transformer energization in the power system are presented

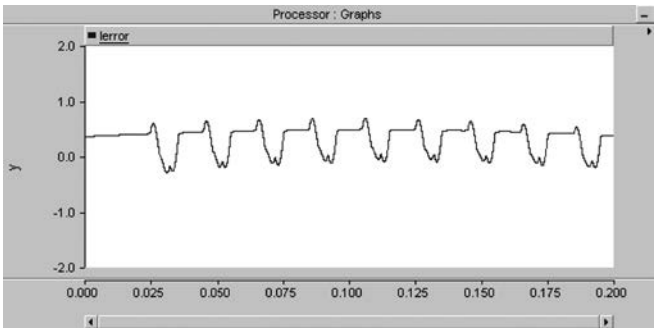

Fig 12.error signal due to transformer energization

In this error signal deviates from zero shortly after the event has been occurred and returns to the steady state when the PLL has been adapted to new conditions

CONCLUSION :

In this paper by taking the implementation of PLL and PSCAD system the work presented in the paper is taken from the theoretical calculations and computer simulations of three phase faults, transformer energization And capacitor energization simulations have been performed using a test system where faults and switching transients have been simulated. For all of these events, a large difference was observed in the error signal of the PLL when a fault or a switching transient was applied. This difference can be used to discriminate faults from switching transients.

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