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Single Stage Step-up/Step-down DC-AC Converter Using Bipolar Modulation

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Abstract
Single stage Buck/Boost inverter is an converter which performs two actions in a single stage. It boosts the DC voltage and invert to AC in a single stage. In Conventional two stage converter there will be two stages. The first stage will be a boost or buck-boost DC-AC converter which is meant for conditioning and leveling the DC voltage approximately to invert to AC voltage required. The second stage will be an inverter, to invert the DC output obtained from first stage to AC voltage. This paper presents a new step-up/step-down DC-AC converter which is having application where an instantaneous voltage higher or lower than input DC voltage is required. It consists of one switching cell including two switches, two diodes, one inductor, and one capacitor on each inverter leg. The PWM is achieved by comparing a high frequency carrier (triangular) waveform with a suitable reference waveform (Sinusoidal). Since the components is less, It makes the system more compact, reliable, less weight, low cost etc. For the Validation of the theoretical analysis, the inverter was simulated for an output rated power of 1 kW, a DC input voltage of 96Vdc and output voltage of 110Vrms. Further, the fundamental output frequency was at 50 Hz and the switching frequency at 20 kHz. Detailed analysis and design of proposed converter is carried out. Simulation results are revealed for circuit validation.
Keywords: *Single stage inverter, Bipolar modulation Buck-Boost converter, Sine PWM control.*

1. Introduction

The rate at which the demand of electrical energy increasing is high now. Conventional sources cannot meet these much demand. So there is a greater depend on non-conventional sources. When depending non- conventional sources , it leads to the development of efficient and low cost power conditioning units to serve as an interface between source and grid. So PCU forms an integral part in power conversion system. Depending on the voltage level, the PCU may be required to “buck” or “boost” the available dc voltage to meet the grid voltage requirements. Depending on the number of power stages used, a PCU may be a single stage or multi stage configuration. For example, Using the buck inverter configuration, proposed by Yang and Sen. [5], power can be fed into the grid from a source whose voltage is greater than the peak grid voltage. Some other two-stage topologies have been proposed [6] which consist of a buck–boost converter cascaded in series with an H-bridge inverter operating at the grid frequency and providing sinusoidal power to the grid. Other two-stage topologies [7], [8] consist of a boost converter stage cascaded with an H-bridge inverter.

In spite of all the advantages offered by a two stage PCU, the presence of more number of power stages undermines the overall efficiency, reliability and compactness of the system besides increasing the cost. Therefore, today the trend is towards the integration of the various stages of a multistage PCU into a single-stage system with as many desirable features of multistage systems [9], [10] as possible. Though a single-stage PCU offers reduced control options (resulting in increased control complexity), these configurations have the advantages of low cost, high efficiency and reliability, modularity, and compactness.

It is not surprising that the single-stage topologies are becoming increasingly popular as compared to the two stage units, particularly for interfacing nonconventional energy sources with the grid. The single-stage buck inverter operation is typically achieved by a simple H-bridge inverter [14]–[16]. However, in order to ensure sinusoidal power output, the converter must be operated with pulse width modulation (PWM) technique which requires switching of the devices at high frequency. This leads to higher switching losses. Also, in this configuration, the source directly supplies energy to the grid through an inductor during the switch-ON interval. Thus, there is no isolation between the

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source and the grid. Many single-stage buck–boost inverter configurations have also been proposed [10], [17], [18]. These configurations feed sinusoidal power into the grid with lower total harmonic distortion (THD) in the grid current and interface nicely with the grid. They also provide an inherent isolation between the source and the grid in the sense that there is an inductor that stores the energy from the source during switch-ON interval and delivers it to the grid during OFF interval without any direct connection between the source and the grid. However, the buck–boost inverter configurations suffer from high peak inductor current stress which is a result of the fact that the entire energy that is transferred to the grid in a switching cycle is stored in the inductor during the ON time of the switching cycle and only this stored energy is supplied to the grid during the OFF time of the switching cycle. This restricts its use to low power applications.
Taking a cue from the above observations, this paper presents a new single-stage inverter topology. Due to the simple structure and low control complexity of the new converter, it is used in applications where an instantaneous voltage higher or lower than input DC is required.

2. Proposed circuit configuration

The block diagram of the proposed converter is shown in Fig.2.1. It consists of an input DC voltage source which is fed to the buck/boost converter .The gate signals for the switches in the inverter is obtained through Bipolar modulation.

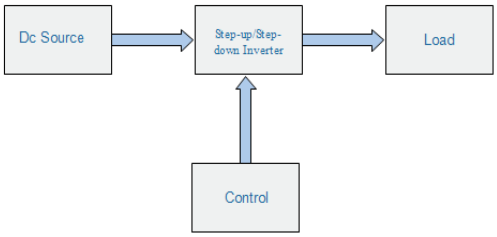

Fig. 2.1 Block diagram of the proposed converter

In sinusoidal pulse width modulation there are two methods: Unipolar modulation and Bipolar modulation. In unipolar modulation the pulses are obtained only in positive direction. But in bipolar modulation pulses are obtained in both positive and negative cycle. Bipolar modulation is one of the technique among sinusoidal pulse width modulation. In bipolar modulation the pulses are obtained by comparing a high frequency carrier signal with a low frequency sinusoidal signal which is the modulating or reference signal. Switching signals are generated by comparing a high frequency triangular waveform (Vp(t)) with the control voltage Vcontrol (Vc(t)). The control voltage is a modulating sine waveform.

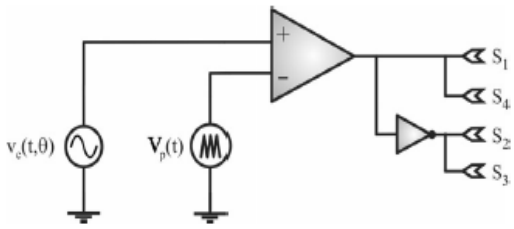

Fig. 2.2 Representative scheme of bipolar modulator

The output power stage of converter is shown in Fig. 2.3. It consists of an input voltage source Vi, a load resistance R_0, two switching cells with elements S_1 ,D_1,C_1,S_2 ,D_2 and L_1 on one cell and S_3,D_3,C_2,S_4,D_4 and L_2 on another cell and a high frequency filter with L_F and C_F.

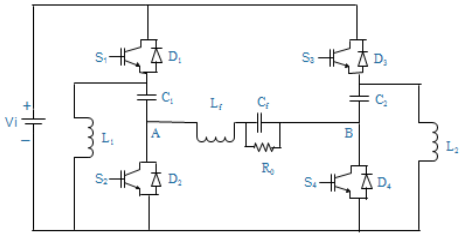

Fig. 2.3 Output power stage of converter

3. Operation principle and waveforms

The complete operation of the converter is divided into two parts on the basis of duty cycle higher than 0.5 and lower than 0.5. The equivalent circuits for duty cycle higher than 0.5 and lower than 0.5 is shown in Fig.3.1. According to the opening and closing of switches there will be two stages on stage and off stage. The on stage corresponds to the closing of switches S_1 and S_4 and off stage corresponds to the opening of switches S_1 and S_4. The switching pulses

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for S_1 and S_4 is same whereas for S_2 and S_3 is just the complementary of S_1 and S_4.

Mode 1: During on stage, when the switches S_1 and S_4 is closed at time t=0 the full input voltage appears across the inductor L_1. After time t increases the current through inductor L_1 starts rising whereas the voltage across it starts decreasing. This voltage starts appearing across the another closed path where this voltage plus the gradually discharging voltage of capacitor makes the voltage at the output higher than that of input. The input current, which rises flows through capacitor C_1, filter inductor L_f, filter capacitor C_f, and load resistor R_0. At the same time the capacitor C_2 discharges its voltage to the inductor L_2 so that the current through inductor L_2 starts increasing.

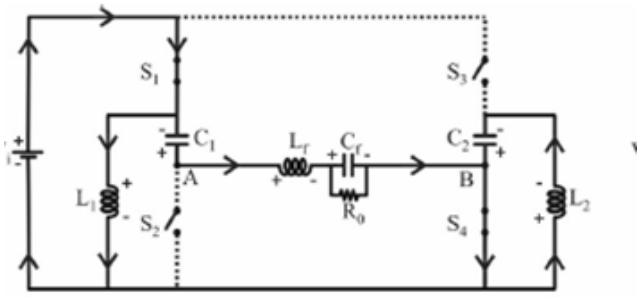

Fig. 3.1 Mode 1

Mode 2: During off stage, when the switches S_1 and S_4 is off the early charged inductor L_2 get discharged towards the source. The early charged inductor L_1 gets discharged through the capacitor C_1 thereby this capacitor C_1 gets charged.

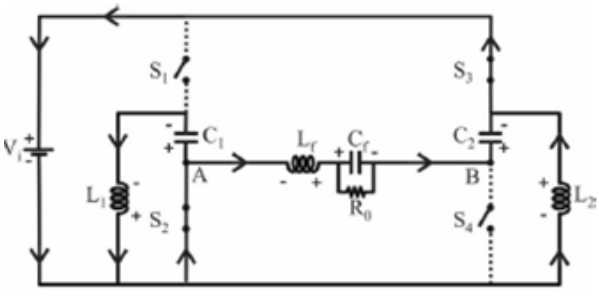

Fig. 3.2 Mode 2

On comparing the waveform it is obtained that the equivalent circuits for the two cases are similar only the current direction through all the elements is reversed. Since the current direction reverses through all the elements in effect the two circuits are same so for an extended analysis we are considering only the circuits for duty cycle higher than 0.5.

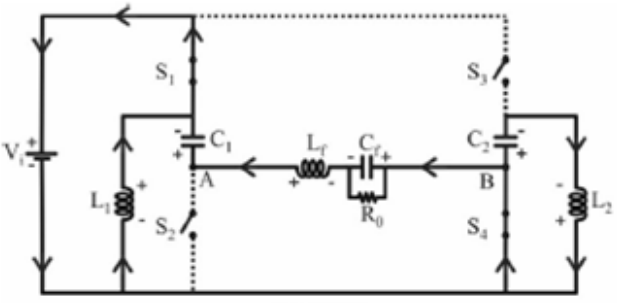

Fig. 3.3 Mode 3

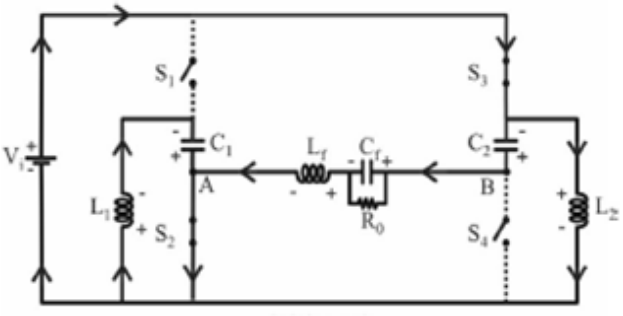

Fig. 3.4 Mode 4

Fig. 3.5 shows the voltage between terminals A and B, the voltage across capacitor C_f, the current across inductor L_f and the command signals applied to switches S_1, S_4, S_2, and S_3. Inductor voltage, current through L_1, L_2 and input current and the command signals applied to switches S_1, S_4 are shown in Fig.3.6. Capacitor voltage, current through C_1, C_2 and the command signals applied to switches S_1, S_4 are shown in Fig. 3.7.

4. Theoretical Analysis

The functions involved in each operation stage and their respective equations are obtained for a fixed duty cycle considering one switching period and steady-state analysis, since transitory conditions and/or load variations were not considered. Table 1 shows the parameters and the mathematical functions for each variable of interest considering all operational stages and a duty cycle d higher than 0.5. These functions are sufficient to evaluate the instantaneous average values for the capacitor voltages and inductor currents.

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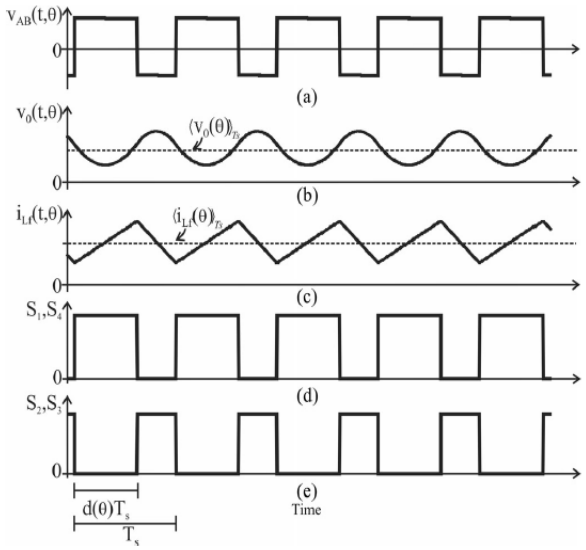

Fig. 3.5 Simulation waveforms: (a) voltage between terminals A and B; (b) voltage across capacitor C_f ; (c) current through inductor L_f ; (d) command signal applied to switches S_1 and S_4 ; (e) command signal applied to switches S_2 and S_3 .

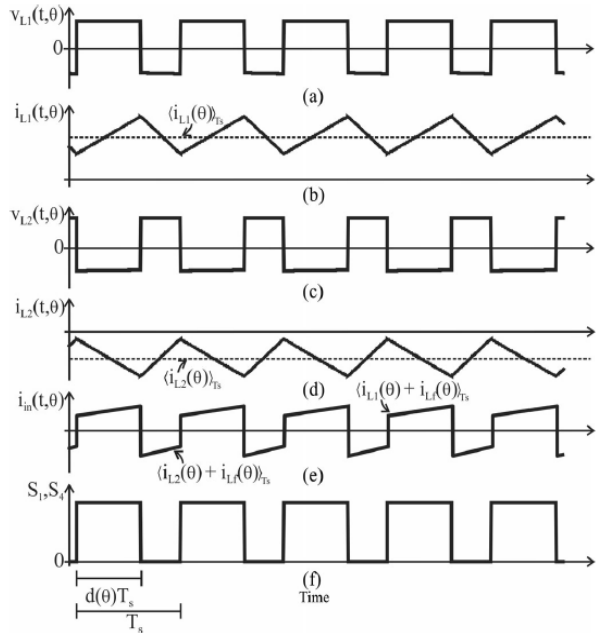

Fig. 3.6 Simulation waveforms: (a) voltage across inductor L_1 ; (b) current through inductor L_1 ; (c) voltage across inductor L_2 ; (d) current through inductor L_2 ; (e) input current; (f) command signal applied to switches S_1 and S_4 .

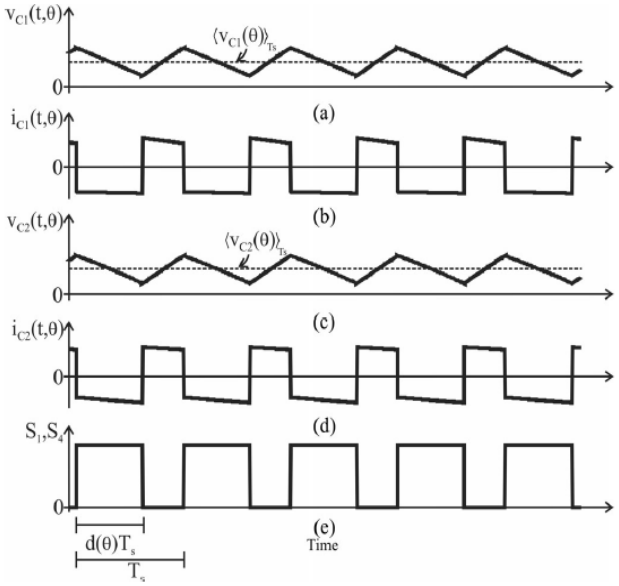

Fig. 3.7 Simulation waveforms: (a) voltage across the capacitor C_1 ; (b) current through capacitor C_1; (c) voltage across the capacitor C_2; (d) current through capacitor C_2; (e) command signals applied to switches S_1 and S_4 .

Table 1: Parameters and indicative functions for the stage of operation

Parameters	**Stage 1**	**Stage 2**
Time interval	dTs	[1-d]Ts
Inductor(L_1) voltage	V_i	$-\langle V_{C1}\rangle_{Ts}$
Inductor(L_2) voltage	$-\langle V_{C2}\rangle_{Ts}$	V_i
Capacitor (C_1) current	$-\langle i_0\rangle_{Ts}$	$\langle i_{L1}\rangle_{Ts}$
Capacitor (C_2) current	$-\langle i_{L2}\rangle_{Ts}$	$\langle i_0\rangle_{Ts}$
V_{AB} voltage	$[V_i + \langle V_{C1}\rangle_{Ts}]$	$-[V_i + \langle V_{C2}\rangle_{Ts}]$

4.1 Voltage across Inductor L_1:

Average voltage across Inductor L_1 over a period

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$$\langle V_{L_1}\rangle T_S = \frac{1}{T_S}\left\{V_{L_1}^{(1)}.dT_S + V_{L_1}^{(2)}[1-d]T_S\right\} \quad (1)$$

Substituting the values of V_{L_1} for each stages from the Table 1.
During stage 1 V_{L_1} is V_i
During stage 2 V_{L_2} is $\langle V_{C_1}\rangle T_S$

$$\langle V_{L_1}\rangle T_S = \frac{[V_i dT_S] + -\langle V_{C_1}\rangle T_{S[1-d]T_S}}{T_S} \quad (2)$$

Average voltage in Capacitor C_1

$$\langle V_{C_1}\rangle T_S = \text{Vi}\left[\frac{d}{1-d}\right] \quad (3)$$

4.2 Voltage across Inductor L_2:

Average voltage across Inductor L_2 over a period

$$\langle V_{L_2}\rangle T_S = \frac{1}{T_S}\left\{V_{L_2}^{(1)}.dT_S + V_{L_2}^{(2)}[1-d]T_S\right\} \quad (4)$$

Average voltage in Capacitor C_2

$$\langle V_{C_2}\rangle T_S = \text{Vi}\left[\frac{1-d}{d}\right] \quad (5)$$

4.3 Current through Capacitor C_1:

Average current through Capacitor C_1 over a period

$$\langle i_{C_1}\rangle T_S = \frac{1}{T_S}\left\{i_{C_1}^{(1)}.dT_S + i_{C_1}^{(2)}[1-d]T_S\right\} \quad (6)$$

Average current through Inductor L_1

$$\langle i_{L_1}\rangle T_S = \langle i_0\rangle T_S\left[\frac{d}{1-d}\right] \quad (7)$$

4.4 Current through Capacitor C_2:

Average current through Capacitor C_2 over a period

$$\langle i_{C_2}\rangle T_S = 0 = \frac{1}{T_S}\left\{i_{C_2}^{(1)}.dT_S + i_{C_2}^{(2)}[1-d]T_S\right\} \quad (8)$$

Average current through Inductor L_2

$$\langle i_{L_2}\rangle T_S = -\langle i_0\rangle T_S\left[\frac{1-d}{d}\right] \quad (9)$$

4.5 Static Gain:

The static gain is determined by the relation between the average voltage V_{AB} and the input voltage V_i

$$\frac{\langle V_{AB}\rangle T_S}{v_i} = \langle q\rangle_{T_S} = \left[\frac{(2d-1)}{d(1-d)}\right] \quad (10)$$

4.6 Voltage Ripple and Current Ripple:

The ripple currents and voltages are presented in Table 2.

Table 2: Ripple current through inductors and ripple voltage across capacitors

Parameter	Current/Voltage Ripple
Ripple Current through Inductor L_1	$\Delta i_{L_1} = \frac{V_i}{L_1}.dT_S$
Ripple Current through Inductor L_2	$\Delta i_{L_2} = \frac{V_i}{L_2}.[1-d]T_S$
Ripple Voltage across Capacitor C_1	$\Delta v_{c_1} = \frac{i_0}{C_1}.dT_S$
Ripple Voltage across Capacitor C_2	$\Delta v_{c_2} = \frac{i_0}{C_2}.[1-d]T_S$
Ripple Current through Inductor L_F	$\Delta i_{L_F} = \frac{V_i}{L_F}.T_S$
Ripple Current through Capacitor C_F	$\Delta v_{c_F} = \frac{1}{8}.\frac{V_i}{L_F C_F}.T_S^2$

4.7 Consideration regarding the new converter operation$_2$:

Due to the nonlinear characteristic inherent to the static gain of the new inverter, it can be concluded that as the duty cycle increases the static gain increases substantially, as highlighted in the static gain curve presented in Fig 3.8. Thus, the application of an increase in the cyclic ratio imposes a large increase in the gain, leading to a distortion in the output voltage of the converter. As a solution for this particularity, the desired voltage gain is used as the reference signal, which is applied at the input of the

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mathematical block, denominated by *F*. The signal obtained at this function output is the operating duty cycle, and it enables the linearization of the relation between the desired static gain and that obtained at the converter output. The following equations show the steps applied to obtain the mathematical block that allows the representation of a sinusoidal output voltage with low distortion, independently of the desired voltage gain. The static gain of the new inverter topology is defined as follows:

$$d = \frac{(\langle q \rangle T_S - 2)}{2.\langle q \rangle T_S} \pm \frac{\sqrt{(4+\langle q \rangle^2 T_S)}}{2.\langle q \rangle T_S} \quad (11)$$

So from this duty cycle is obtained as a function of static gain. So the function given in the block F is

$$F = \frac{(\langle q \rangle T_S - 2)}{2.\langle q \rangle T_S} \pm \frac{\sqrt{(4+\langle q \rangle^2 T_S)}}{2.\langle q \rangle T_S} \quad (12)$$

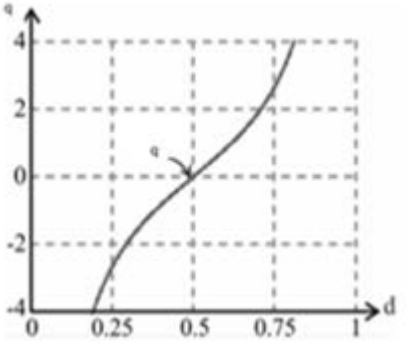

Fig. 3.8 Static gain in function of duty cycle

5. Design Example

The main purpose of this section is to use the previously deduced equations to calculate the components value.

5.1 Specifications:

Po	1kW (output power)
Vo	110 Vrms (output voltage)
Vin	96Vdc (input voltage)
Fo	50 Hz (output voltage frequency)
Fs	20kHz (switching frequency)
q	1.61(maximum static gain)

5.2 Calculation of duty cycle:

The maximum static gain is 1.61. Substituting these in Eq (12) maximum duty cycle obtained is 0.68.

5.3 Calculation of L_1 and L_2:

The maximum inductor current ripple $\Delta i_{L_1\,max}$ is chosen to be equal to 50% of maximum inductor current. The inductor current i_{L_1} is obtained from (7). From the equation shown in Table Δi_{L_1} is obtained. Substituting $i_{L_1 max} = i_{L_1}$ one obtain $L_1 < 300\mu H$. $L_1 = 255\mu H$ is adopted. L_2 is same as L_1.

5.4 Calculation of C_1 and C_2:

The maximum capacitor voltage ripple $\Delta V_{C_1\,max}$ is chosen to be equal to 40% of maximum capacitor voltage. From these ΔV_{Cf} is 437.104V. On substituting these the obtained C_1 is 1 µF. C_2 is same as C_1 as 1 µF.

5.5 Calculation of L_f and C_f:

An inductor is used in a filter to reduce the ripple current. This reduction occurs because current through the inductor cannot change suddenly.

$$F_c = \frac{1}{2\Pi\sqrt{L_F C_F}} \quad (13)$$

Eqn (13) shows the equation for finding critical frequency (F_c). But F_C is normally 5%-25% of switching frequency. By using (13) L_F is found out .C_F is assumed to be 5µF.. From this one obtains L_F < 2mH.The adopted L_F is 1.5mH.

5.6.Calculation of R_0:

With the equation power = $v_{rms} \times i_{rms}$ the current i_0 can be found.

$$v_0 = i_o \times R_o \quad (14)$$

The adopted Ro is 12Ω.

6. Simulation Analysis and Results

In power stage four MOSFET switches are used. Proposed circuit is simulated with open loop control, in which, output voltage is controlled by varying amplitude of the reference sine wave, in effect duty

cycle, D, corresponding to maximum value of output voltage. With Vo = 110V_{rms},Vi = 96V_{dc}, R = 12Ω, Fs = 20kHz as per design equations value of inductor is obtained as L_1, L_2 = 255 μH and value of capacitors C_1, C_2 is obtained as C = 1μF. Inorder to eliminate high switching frequency component from output voltage, cutoff frequency of output filter is decided as 1800Hz. Then filter inductor is obtained as L_f = 1.5 mH.Fig.6.1 shows output voltage is a pure sinusoidal waveform and the output voltage is about 110 Vrms.

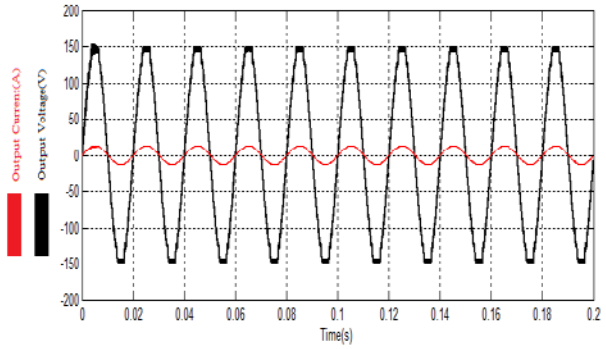

Fig. 6.1 Output voltage and current waveform for R load

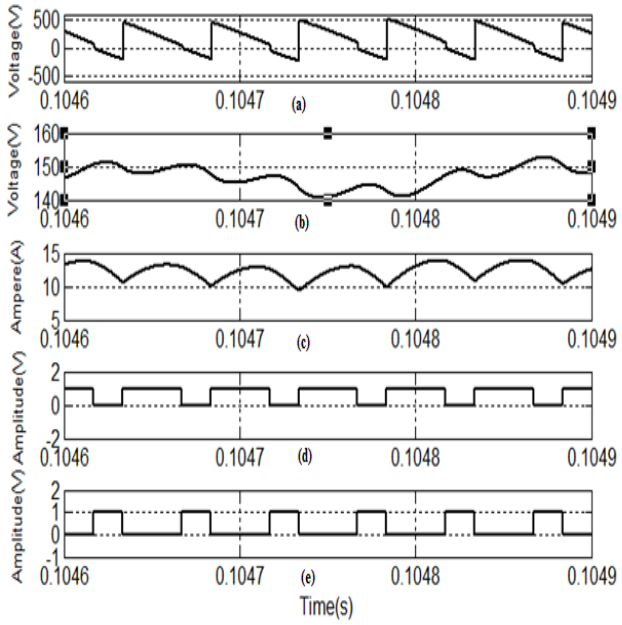

Fig. 6.2 Simulation waveforms 1: (a) voltage between terminals A and B; (b) voltage across capacitor C_f ; (c) current through inductor L_f ; (d) command signal applied to switches S_1 and S_4; (e) command signal applied to switches S_2 and S_3.

Fig. 6.2 (a) shows that During mode 1 the voltage across the terminals A and B starts decreasing in the positive direction whereas during off time voltage starts increasing in negative direction. Fig. 6.2 (b) shows that the output voltage is a pure sinusoidal waveform. Fig. 6.2 (c) shows that the current across inductor is firstly increases and then decreases linearly. When switches S_1 and S_4 is on, current increases and reaches a final value. When switches S_1 and S_4 is off current across inductor decreases from its final value. This is the case when duty cycle greater than 0.5. When duty cycle is below 0.5, current starts increasing in negative direction during switches S_1 and S_4 is on. When off current starts decreasing from the negative side. Fig. 6.2 (d) shows the pulses given to switch S_1 and S_4. The compliment of above pulse is for switch S_2 and S_3. For producing these pulses triangular wave compared with a duty ratio waveform and then given to relational operator. When the amplitude of duty ratio waveform is higher than that of triangular wave, pulses are generated.

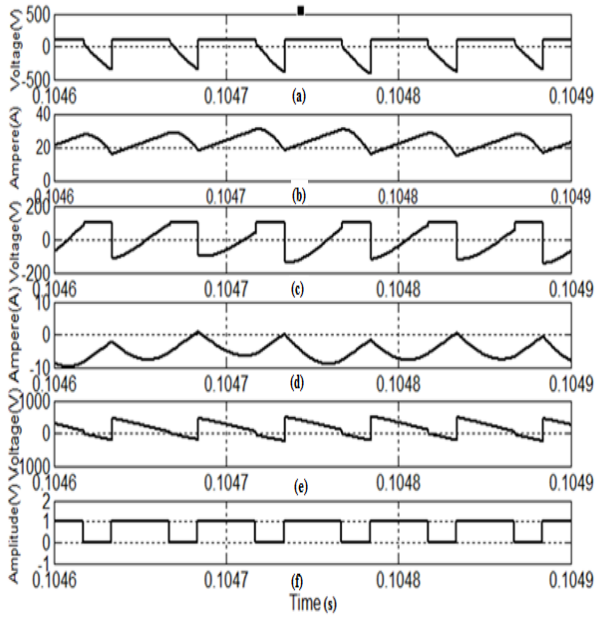

Fig.6.3 Simulation waveforms 2 : (a) voltage across inductor L_1 ; (b) current through inductor L_1 ; (c) voltage across inductor L_2 ; (d) current through inductor L_2 ; (e) input current; (f) command signal applied to switches S_1 and S_4.

Fig.6.3 (a) shows that the voltage is positive during Switches S_1 and S_4 is on. At that time current is increasing and reaches final value. When switches S_1 and S_4 is off the voltage starts increasing in the negative direction where as current starts decreasing. Fig.6.3 (c) shows that the voltage is negative and starts increasing during on time and positive remains constant during off time and the current is decreasing and then increasing and it is negative too. Fig..6.4 (a) shows that the voltage is positive during Switches S_1 and S_4 is on. At that time current is increasing and reaches final value. When switches S_1 and S_4 is off the voltage starts increasing in the negative direction where as current starts decreasing. Fig.6.4 (c) shows that the voltage is negative and starts increasing during on time and positive remains constant during off time and the current is decreasing and then increasing and it is negative too.

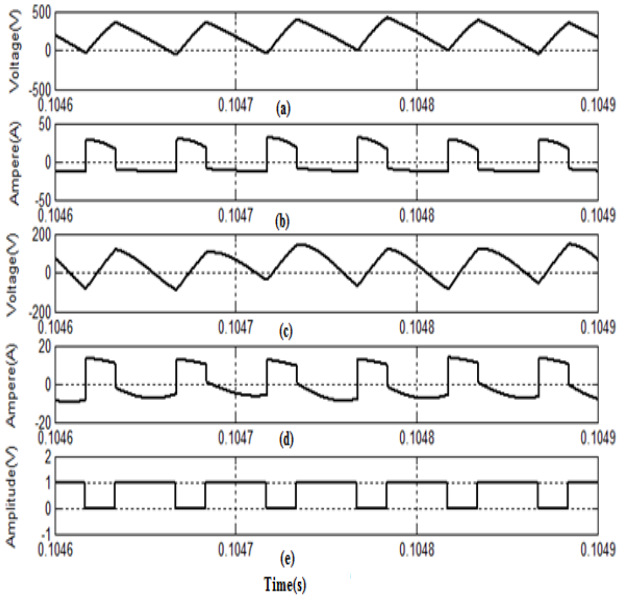

Fig. 6.4 Simulation waveforms 3: (a) voltage across the capacitor C_1 ; (b) current through capacitor C_1 ; (c) voltage across capacitor C_2 ; (d) current through capacitor C_2 ; (e) command signals applied to switches S_1 and S_4.

7. Conclusion

This paper presented a new topology for dc–ac converters whose main feature is its capacity to provide an instantaneous output voltage higher or lower than the input voltage without an intermediate power stage or transformer. The circuit configuration of proposed converter is very simple and it is modified form of the Buck-Boost inverter. The advantages of the circuit are low cost, high efficiency, low component counts etc. Analysis and design of the overall system were discussed. In future the system can be made to closed loop by using any feedback controller. The closed loop control improve system dynamic response and it provides a good regulated output voltage.

Based on theoretical analysis and simulation results the following conclusions can be drawn:

1) The evaluated performance was in agreement with the theoretical analysis;

2)The converter provide both buck and boost operations .

3) It can be used in applications where instantaneous voltage higher or lower than DC voltage is required.

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