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Closed Loop Analysis of a High Efficient Single Stage Power Factor Correction (SSPFC) Converter

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Abstract
High power factor and low input current harmonics are more and more becoming mandatory performance criteria for power converters so that they meet agency standards. In this paper, a new Single stage power factor correction AC–DC converter with asymmetrical pulse width is presented. The proposed converter integrates the operation of the boost power factor correction and the three-level DC–DC converter. The converter is made to operate with two independent controllers -an input controller that performs power factor correction and regulates the DC bus and an output controller that regulates the output voltage. The outstanding feature of this converter is that it combines the performance of two-stage converters with the reduction of cost of single-stage converters. Simulation was done in MATLAB/Simulink and results were verified for closed loop operation of converter.
Keywords: *AC-DC power conversion, Single-stage power factor correction(SSPFC), three level converters.*

1. Introduction

AC-DC converters are typically used in many industrial and commercial applications like personal computers, battery chargers, telecommunication power supplies, etc. Switch mode AC-DC converters are the first block in any power conversion system that supplies power from an AC source such as the utility mains to any load. An AC-DC power supply should operate in such a way that the input current and voltage are purely sinusoidal and in phase with each other to comply with harmonic standards and thus ensure a good input power factor. As a result, power factor correction (PFC) techniques are typically used in AC-DC power converters to ensure that these standards are met. Switch mode AC/DC converters are the first building block to supply power from AC mains to downstream converters for the electronics circuits, normally known as loads. So, they should provide performance characteristics that are acceptable by both the AC mains and the output load. From the AC mains point of view, a power supply should provide good power quality such that the input current and input voltages are purely sinusoidal at the line frequency and are in phase. Whereas, from the load point of view, a well regulated output voltage with low ripples is required. In order to conserve energy, high overall power conversion efficiency is required. However, conventional AC/DC switch mode power supplies introduce some adverse effects on the AC side. Examples of such effects are distortion of input current or voltage, input voltage dip due to the presence of bulk capacitors and electromagnetic interference due to high frequency switching. In recent year's power factor correction circuitry have become integral part of the AC/DC power supply design to meet the input power quality requirements. The PFC circuits also can be used to regulate output voltage and that can also improve the conversion efficiency. There are two main methods to eliminate the input line current harmonics:

1. Passive power factor correction - A series tuned passive LC filter at the fundamental operating frequency is a suitable way for obtaining unity power factor in high frequency AC power distribution systems. Advantages of this method are high efficiency, low EMI and simple implementation.
2. Active power factor correction - Here, switching converters are used to shape the input current drawn by the AC/DC converter into a sinusoidal waveform that is in phase with the input voltage waveform.

2. Literature Survey

Several SSPFC topologies have been introduced in the literature, but these single stage converters had limitations on their output power and the range of input voltage. Previously proposed single stage AC-

DC full bridge converters can be classified as belonging among the following types:

2.1 Current fed converters

Although it is possible to satisfy the harmonic standards by adding passive filter elements to the traditional passive diode rectifier/LC filter input combination as in a conventional PWM converter, the resulting converter would be very bulky due to the size of the low-frequency inductors and capacitors [1]. The passive diode rectifier/LC filter input combination can be replaced with a boost converter in the rectifying stage. It shapes the input line current so that it is almost sinusoidal, with a harmonic content compliant with agency standards, but the cost and complexity of the overall two- stage converter are increased.

Converters that integrate the PFC and DC–DC conversion functions in a single switching converter have been proposed shown in Fig 2.1 [2]. This results in cost savings due to the elimination of the boost converter switch and the controller used to control its operation. However, it has several drawbacks, one of these being the lack of an energy storage capacitor across the primary-side DC bus. This results in the appearance of high voltage overshoots and ringing Across the DC bus whenever a converter switch is turned off, requiring that higher voltage rated devices are used for the converter switches. Another drawback with the converter topology is that the output voltage has a large low-frequency 120-Hz ripple that restricts the use of this converter to applications where a tightly regulated output voltage is not required. These problems can be eliminated if a voltage-fed full-bridge converter with output LC filter is used.

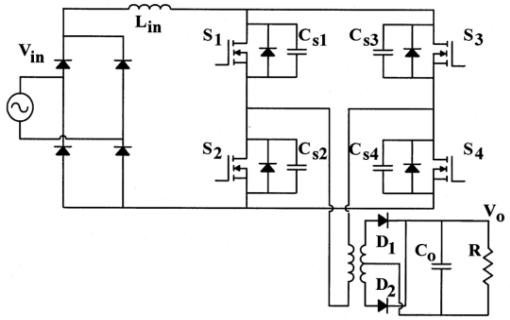

Fig 2.1 Current Fed Converter

2.2 Voltage fed converters

The voltage fed converter in Fig. 2.2 is almost the same as a conventional PWM full-bridge converter with a diode rectifier, L–C filter front-end, except that input inductor is connected to switch instead of energy-storage capacitor. This modification allows switch to perform the same current-shaping function as the switch in a boost converter so that there is no need to add an additional boost converter for PFC; otherwise, the converter operates in a manner similar to a standard PWM full-bridge converter. The bus capacitor prevents voltage overshoots and ringing from appearing across the DC bus and the 120-Hz AC component from appearing at the output.

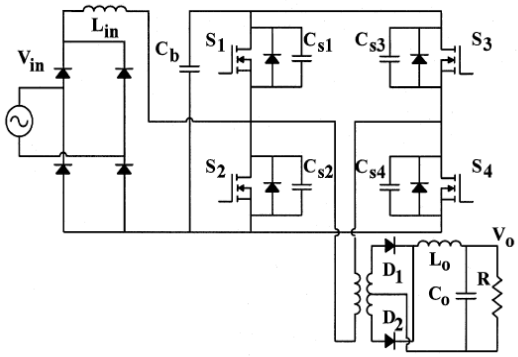

Fig 2.2 Voltage Fed Converter

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Voltage-fed converters, however, have many disadvantages [3]. The primary-side DC-bus voltage of the converter may become excessive under high input- line and low-output-load conditions. This is because SSPFC converters are implemented with just a single controller to control the output voltage, and the DC-bus voltage left unregulated. The high DC-bus voltage results in the need for higher voltage rated devices and very large bulk capacitors for the DC bus. The input power factor of a single-stage voltage-fed converter is not as high as that of current-fed converters. The converter is made to operate with an output inductor current that is discontinuous for all operation conditions or some parts of operation conditions [6], to try to prevent the DC-bus voltage from becoming excessive; output inductor current and DC-bus voltage are related. Doing so results in the need for components that can handle high peak currents and additional output filtering to remove ripple.

2.3 Resonant converters

These converters have resonant elements such as inductors and capacitors that are connected in series or parallel to the primary of their transformer as shown in Fig 2. It solves many problems like high component stresses, high circulating currents, and low efficiency [4]. The drawback is that the efficiency drops as the load is reduced because the converter starts to drift away from its resonance frequency, thus leading to more circulating currents and conduction losses. It must be controlled using varying switching frequency control, which it makes it difficult to optimize their design as they must be able to operate over a wide range of switching frequency [5] [6].

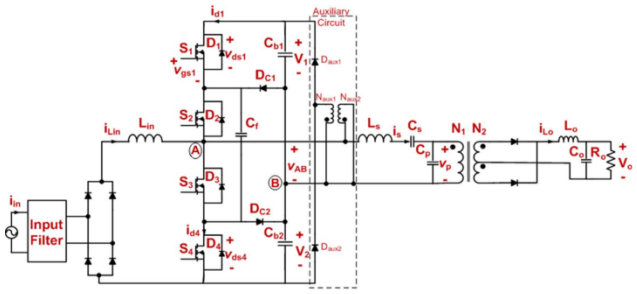

Fig 2.3 Resonant Converter

3. SSPFC Converter With Asymmetrical Pulse Width Modulation

The overall circuit diagram of the converter is showed in Fig 3.1. The proposed converter integrates an AC–DC Boost PFC converter into a three-level DC–DC converter [7]. Asymmetrical pulse width modulation technique is used. Here the operation of this converter is in three levels, in first level we are constructing a diode bridge with boost inductor L_{in} , boost diode D_{x1}, In second level we are using four switches along with two capacitors, named as C_1 and C_2 is used. Switch S_4, is shared by the multilevel DC–DC section. In third level we are using center tapped transformer with half wave diode bridge and inductor L_o is used for DC generation. In first level we are converting input AC into DC by using the full bridge diode bridge operation. In second level we are converting this DC into AC. In this level we are using MOSFETs to convert DC into AC. Because MOSFETs have high switching frequency, When S_4 is off, it means that no more energy can be captured by the boost inductor. In this case, diode D_{x2} prevents input current from flowing to the midpoint of capacitors C_1 and C_2. In this case we are using high switching frequency for MOSFETs i.e. 20 KHz.
Although there is only a single converter; it is operated with two independent controllers. One controller is used to perform PFC and regulate the voltage across the primary-side DC bus capacitors by sending appropriate gating signals to S_4. The other controller is used to regulate the output voltage by sending appropriate gating signals to S_1 to S_4. It should be noted that the control of the input section is decoupled from the control of the AC– DC section and thus can be designed separately.

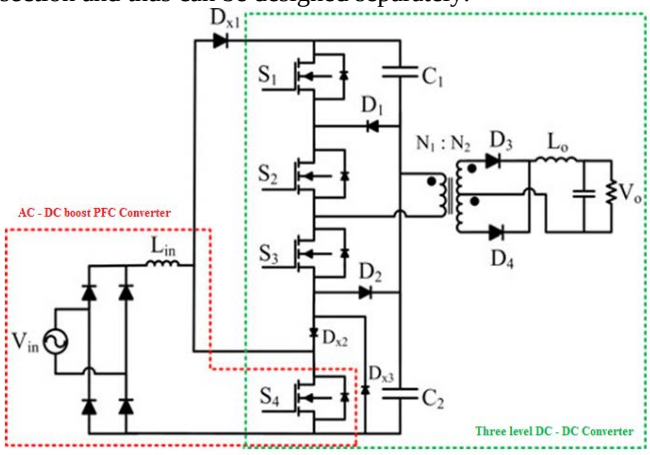

Fig 3.1 Proposed single stage PFC converter

Typical converter waveforms are shown in Fig 3.2, and equivalent circuit diagrams that show the converter's modes of operation are shown in Fig 3.3 to 3.10 with the diode rectifier bridge output replaced by a rectified sinusoidal source.

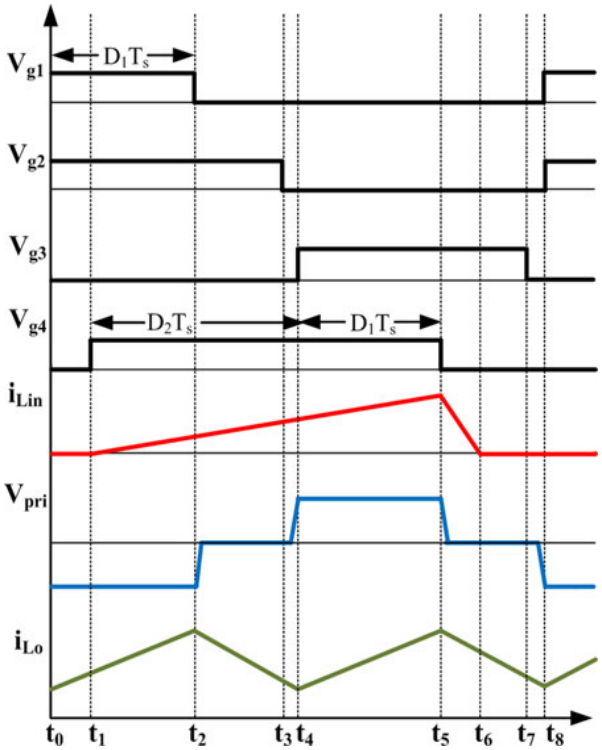

Fig 3.2 Typical waveforms describing modes of operation

Mode1 ($t_0 \le t \le t_1$): During this mode, switches S_1 and S_2 are ON and energy from DC-bus capacitor C_1 is transferred to the output load .

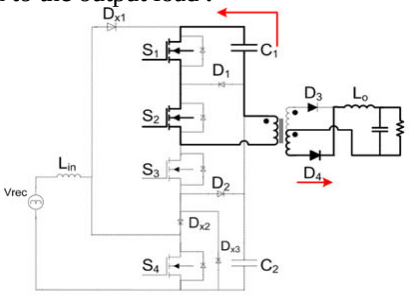

Fig 3.3 Mode 1

Mode 2 ($t_1 \le t \le t_2$): In this mode, S_1 and S_2 remain on and S_4 is turned on. The energy from DC bus capacitor is transferred to load. Also, V_{rec} is impressed across L_{in} so that the current flowing through this inductor rises.

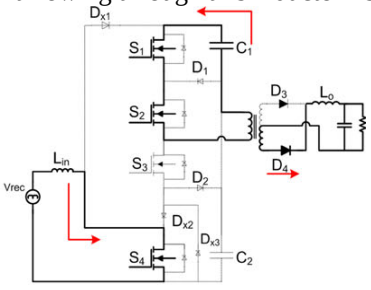

Fig 3.4 Mode 2

Mode 3 ($t_2 \le t \le t_3$): During this mode, S_1 is turned off . The current in the primary of the transformer circulates through D_1 and S_2 and the output inductor current freewheels through the secondary of the transformer.

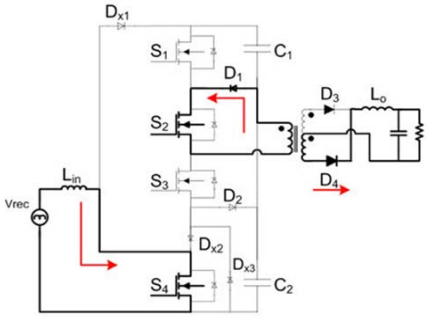

Fig 3.5 Mode 3

Mode 4 ($t_3 \le t \le t_4$): During this mode, switch S_2 is turned off. The current in the primary of the transformer charges capacitor C_2 and output inductor current decreases.

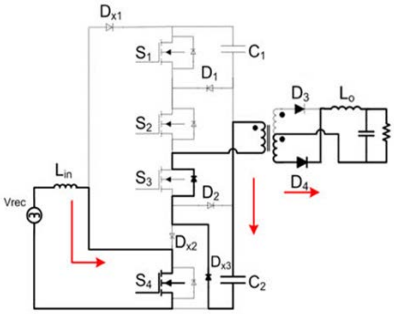

Fig 3.6 Mode 4

Mode 5 ($t_4 \le t \le t_5$): In this mode, switches S_3 and S_4 are on. Energy from capacitor C_2 flows into the load while the current flowing through input inductor L_{in} continues to rise.

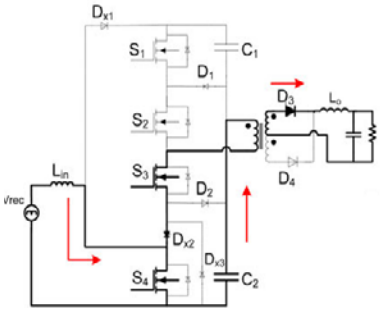

Fig 3.7 Mode 5

Mode 6 ($t_5 \le t \le t_6$): In this mode, switch S_4 is turned off. The current in input inductor flows thorough the diode D_{x1} to charge the capacitors C_1 and C_2. This mode ends when the inductor current reaches zero.

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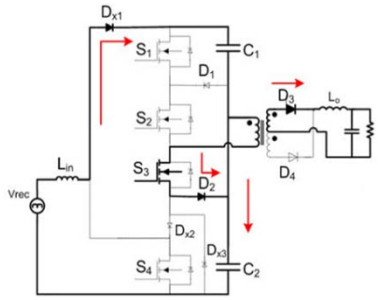

Fig 3.8 Mode 6

Mode 7 ($t_6 \leq t \leq t_7$): In this mode, switch S_3 is on and this mode ends when the switch S_3 is turned off.

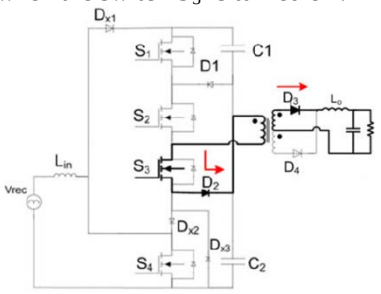

Fig 3.9 Mode 7

Mode 8 ($t_7 \leq t \leq t_8$): S_3 is also turned off and the current in the primary of the transformer charges the capacitor C_1 through the body diodes of S_1 and S_2.

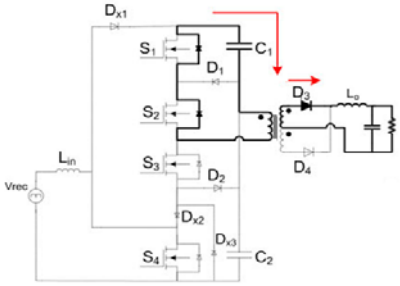

Fig 3.10 Mode 8

4. Design Analysis and Control Circuit

A procedure for the design of the converter is presented in this section. The converter is to be designed with the following parameters as shown in Table 4.1.

Table 1: Design Parameters

Parameters	***Value***
Input voltage	150 V_{peak}
Output voltage	48V
Output power	1350W
Switching frequency	20KH

Step 1: Determine Value for Output Inductor L_o

The output inductor should be designed so that the output current is made to be continuous under most operating conditions. The minimum value of L_o can be determined to be

$$Lo, min \geq \frac{{V_o}^2}{0.5\, P_{o,max}} \frac{1-D_m}{2} \frac{T_{SW}}{2} \quad (1)$$

Substituting $P_{o,max}$ = 1350 W, V_o = 48 V, T_{SW} = 50 µs, and D_m = 0.5 gives $L_{o,min} \geq$ 21 µH and the value of L_o should be larger to provide some margin. A value of L_o = 1000 µH, is chosen.

Step 2: Determine Value for Turns Ratio of Main Transformer N

The minimum value of N can be found by considering the case when the converter must operate with minimum input line and, thus, minimum primary-side DC-bus voltage $V_{bus,min}$ and maximum duty cycle D_{max}.

$$N \geq \frac{V_{bus,min}}{2V_o} . D_{max} \quad (2)$$

where V_o = 48 and D_{max} = 0.5, V_{bus} = 650 V then the value of N should be equal or more than 3.3. The value of transformer ratio is considered to be equal to N = 5.

Step 3: Determine Value for Inductor L_{in}

The value for L_{in} should be low enough to ensure that the input current is fully discontinuous under all operating conditions, but not so low as to result in excessively high peak current. The minimum value of L_{in} determine as

$$L_{in,max} < \frac{[(V_{bus,min})]^2 * D_{max} * (1-D_{max})^2}{2P_{o,max} f_{sw}} \quad (3)$$

where D_{max} = 0.75, $V_{bus,min}$ = 650 V, $P_{o,max}$ = 1.35 kW, and f_{sw} = 20 kHz. The minimum value of L_{in} = 285 µH is found. Here, L_{in} = 60 µH is used.

Step 4: Determine load resistance R

$$R = \frac{{V_o}^2}{P} \quad (4)$$

Substituting Vo = 48V and P = 1350W, R is calculated to be 1.706Ω.

There are two PI controllers as shown in Fig 4.1. One is to control DC–DC conversion of the DC-bus voltage to the desired output voltage, and this can be done by controlling the gating signals of S_1 to S_4 through controlling duty cycle of D_1. The other is to control duty cycle of the switch S_4 to regulate the DC-bus voltage and to perform input power factor correction. This can be done by controlling D_2 and then adding duty cycle of D_2 to D_1.

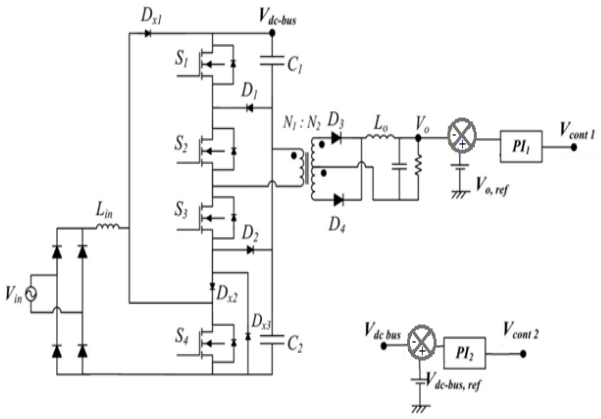

Fig 4.1 Control Circuit

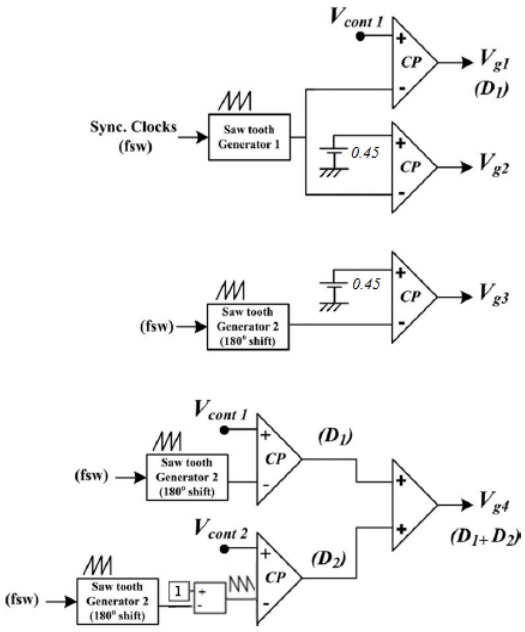

Fig 4.2 Formation Gating Signals

The formation of gating signals are as shown in Fig 4.2 from D_1 and D_2 obtained from the controllers. There are two saw tooth generators, one having a phase shift of 180^0 with the other. The phase shifted saw tooth wave is subtracted from 1 in order to get an inverted phase shifted saw tooth wave. D_1 is compared with the saw tooth wave to give switching pulse, V_{g1} to switch S_1. The same D_1 is also with the phase shifted saw tooth to give the pulse a phase shift of 180^o. It is then added with the signal obtained by comparing D_2 with the inverted phase shifted saw tooth wave to give switching pulse V_{g4} for switch S_4.The switching pulses V_{g3} and V_{g4} are produced by comparing two constant blocks of 0.45, one with the saw tooth and other with the phase shifted saw tooth as shown and are given to switches S_2 and S_3. The decoupling of the input controller and output controller can occur because the crossover frequencies of the two loops are very different. It is therefore possible to consider the design of one controller to be separate from that of the other.

5. Closed Loop Simulation and Results

The parameters given for simulation according to the design are shown in Table 7.1 below.

Table 4.3 Closed loop parameters

Parameters	Value
Input inductor	60µH
Bus capacitors	2200 µF
Output inductor	1000 µH
Output capacitor	22000 µF
Load resistance	1.706Ω

Closed loop control of the SSPFC AC-DC converter is simulated in MATLAB/Simulink as shown in Fig 5.1. Here PI controller with trial and error method is used for the closed loop operation. The input current is in phase with the input voltage and has a perfect sinusoidal shape as shown in Fig 5.2 indicating high value of power factor. The power factor was calculated and seen to be 0.996 as shown in Fig 5.3. The output voltage and DC bus voltage take some time to settle to their respective values as shown in Fig 5.4 and 5.5 respectively. The gating signals along with the input inductor current, primary transformer voltage, output inductor current are shown below in Fig 5.6. The closed loop efficiency was calculated to be 92% as shown in Fig 5.7.

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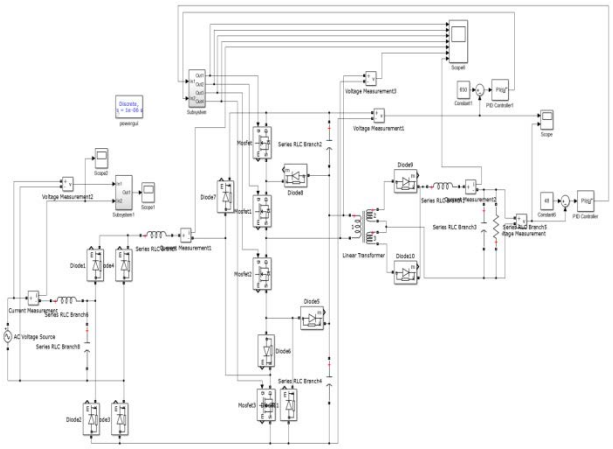

Fig 5.1 Simulation Circuit

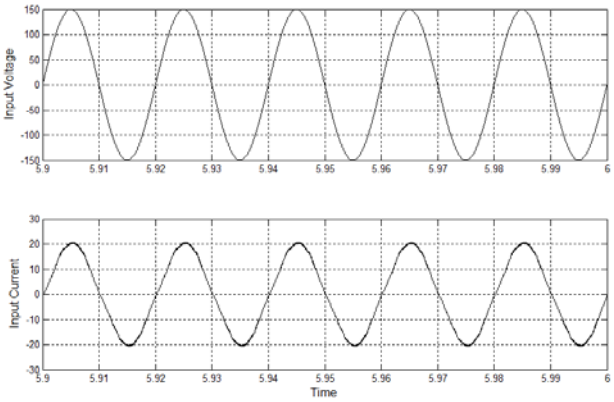

Fig 5.2 Waveform of Input voltage and current

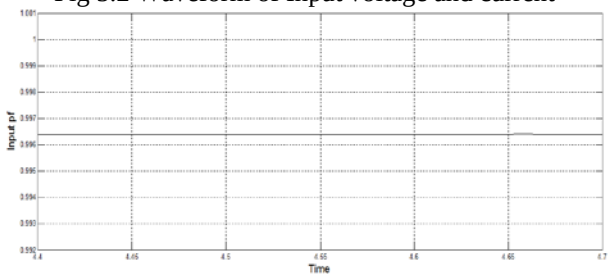

Fig 5.3Iinput power factor

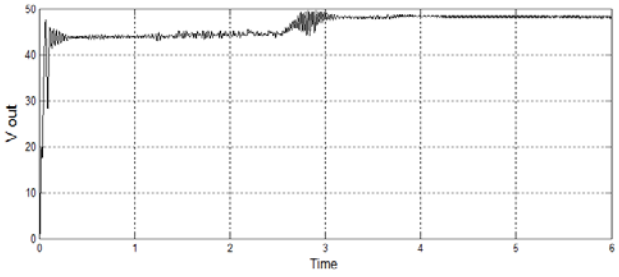

Fig 5.4 Waveform of Output Voltage

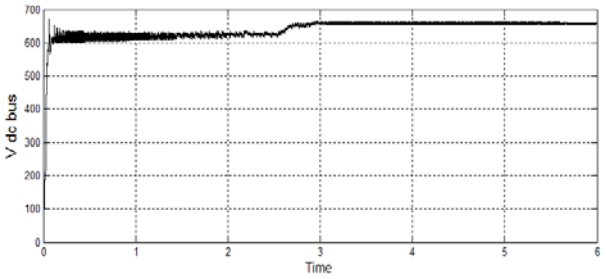

Fig 5.5 Waveform of Primary DC bus Voltage

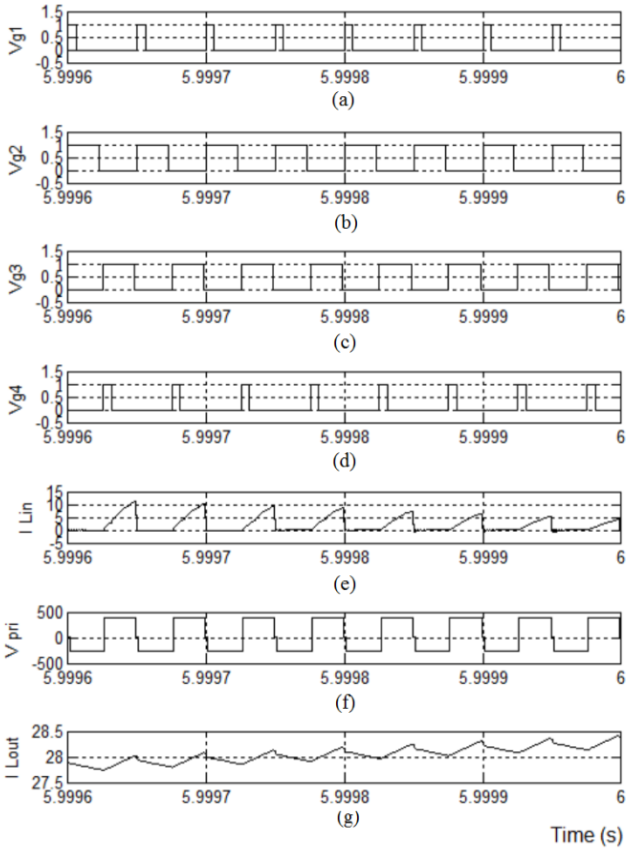

Fig 5.6 Waveforms (a) Gating signal of S_1, V_{g1}; (b) Gating signal of S_2, V_{g2}; (c) Gating signal of S_3, V_{g3}; (d) Gating signal of S_4, V_{g4}; (e) Input inductor current; (f) Transformer primary voltage; (g) Output inductor current

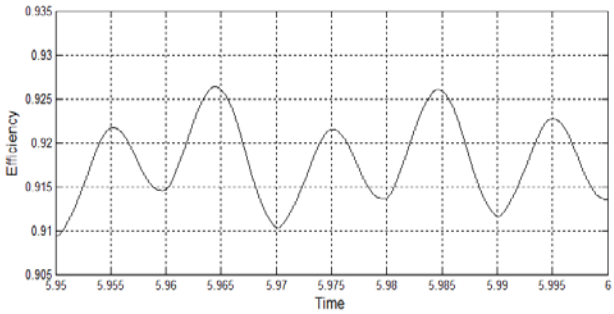

Fig 5.7 Circuit Efficiency

7. Conclusion

A new multi level SSPFC AC to DC converter is proposed in this paper. Simulation of closed loop circuit was done and efficiency of 92% was obtained with high input power factor of 0.996.

Acknowledgments

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