International Journal of Scientific Engineering and Applied Science (IJSEAS) - Volume-1, Issue-4, July 2015
ISSN: 2395-3470
www.ijseas.com

Design of Inter-Integrated Circuit Bus Protocol and by using BIST Method-A Review

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Abstract

The Inter-Integrated circuit protocol is used to attach two devices for communicating with each other in fast way excluding data losses. It can be created by Phillips in the earl's of1980's It can be used to interface low speed peripherals like mother board, embedded system, and mobile phones, set top boxes, DVD and other electronics devices. With the fast development of Integrated circuits (ICs) technology, the complication of the circuits has also increase day by day. To save time and money the circuit requires self -testability in hardware to palliate the product failure. BIST is system develop to performing functional testing at different speed. Built-in-self-test (BIST) is such a technique which can meet the necessity of self-testability with an effective solution over pricy circuit testing system. This synopsis proposed designing of Inter-Integrated Circuit (I2C) protocol with self-testing ability. In order to attain compact, stable and reliable data transmission, the I2C is designed with self-testability is needed.

Keywords

Inter-integrated Circuit, Built-in Self-test Architecture, Verilog HDL.

1. Introduction

The I2C (Inter-Integrated Circuit) is a two-wire bus, which is low to medium speed, communication bus (a path for electronic signals) developed by Philips Semiconductors in the early 1980s.The I2C was develop or created to reduce the manufacturing costs of electronic products.I2C is an bidirectional serial bus, which gives effective data communication between two devices. The actual or physical I2C bus consists of just two wires, which are SCL and SDA. The SCL is a serial clock line; it is used to synchronize the whole data transfers over the I2C bus. Besides that, SDA is the serial data line; it is used to carries the data. The SCL and SDA lines are connected to all devices on the I2C bus. Fig.1 shows the Format of I2C bus protocol bus. [3]

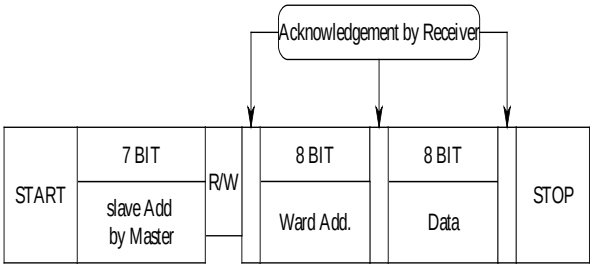


Fig.1: Format of I2C Protocol Bus

- *Start and Stop Conditions*

A change in the state of the serial data line, from HIGH to LOW, during which the clock is HIGH, defines a START condition. And during state of change of the data line, from LOW to HIGH, while the clock line remains HIGH, which defines the STOP condition.

- *Slave Address*

The slave address consists of 7 bit data format. This address is represents the name of the specific device. In which the master determine the address of slave devices where it must be transmits the data.

- *Read/Write bit*

This one bit represents the operation to perform on the slave, while it should be Read or Write. LSB of 1st byte is to be sent. If '1' is sent then it performed a Read operation and if '0' is sent then it performed write operation.

- *Word Address*

The master indicates or tells the slave device the address of data. So, word address is actually like the address bus of the data. It is also an 8 bit data.

- *Data Value*

Data values consist of 8 numerical which are 8 bit long. These are the values which transmit from master to slave. [3].

- *Getting acknowledge (ACK) from a slave device*

When an address or data byte has been transmitted onto the bus then this must be acknowledged by the slave(s). The slave keeps SDA Low during the 9th clock of SCL.

- *Giving acknowledge (ACK) from a slave device*

Upon reception of a byte from a slave, the master must acknowledge this to the slave device. If there is no data left to receive, the master will send a not-acknowledge (NACK) signal and will stop the data transaction.

2. Proposed Work

Built-In Self-Test (BIST), as the name suggests is a technique in which the circuit is capable of testing itself. Testing of Integrated circuit (IC) is of curical importance to ensure a high level of quality in product functionality in both commercially and privately product. Impact of testing affects area of manufacturing as well as those involve in design. BIST test has become a major design consideration in Design For testability method. It reduces testing and maintenance cost and also reduces cost of automatic test pattern generation (ATPG).

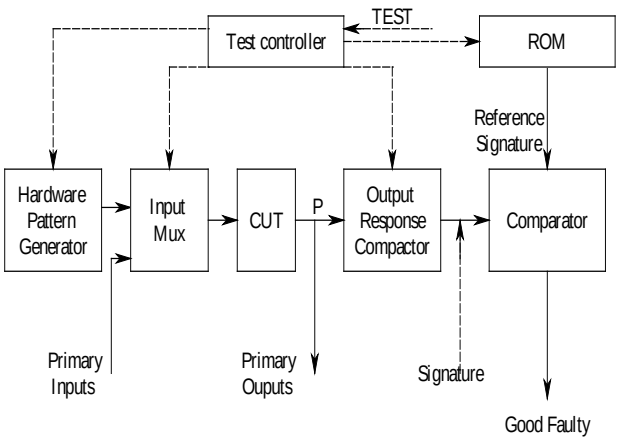


Fig.2: BIST Architecture

BIST is a set of structured- test technique for combinational and sequential logic, memories, multiplier and other embedded logic blocks. Figure shows typical BIST process. The wires from PIs to the Input MUX and the wires from circuit outputs P to primary outputs (POs) cannot be tested by BIST. These wires, instead, require another testing method, such as an external ATE or JTAG Boundary Scan hardware. Figure show the test response of the circuit. Figure also shows how a comparator compares the signature produced by the data compacter with a reference signature stored in a ROM during BIST. The wires from PIs to the Input MUX and the wires from circuit outputs P to primary outputs (POs) cannot be tested by BIST. Figure also shows how a comparator compares the signature produced by the data compacter with a reference signature stored in a ROM during BIST. This comparator and ROM hardware can frequently be implemented with a single logic gate with 32 or fewer inputs.[7].

BIST is an on – chip test logic that is utilize to test the functional logic on chip. It consist of different part such as Test pattern generator (TPG), circuit under test(CUT) and Response analysis. The implementation requires primarily two components: a pseudo-random test patter generator (for test vector generation) and a data compactor (for output response analysis). There is different form of BIST pattern generation. Such as the following hardware pattern generation approaches have been used,

- *ROM*

This method is to store a good test-pattern set (from an ATPG program) in a ROM on the chip, but this method is prohibitively expensive in chip area.

- LFSR

This method is to use a *linear feedback shift register* (LFSR) to generate pseudo-random tests. This requires a sequence of 1 million or more tests to obtain high fault coverage's, and the method uses very little hardware and is currently the preferred BIST pattern generation method.

- Binary Counters

A binary counter this method can generate an exhaustive test sequence, but this method can use too much test time for huge number of inputs. For example, with 64 inputs and the test-pattern generator clocked at 100 *MHz*, this takes 51,240,955.8 hours of test time to generate all patterns,

which is impractical. Therefore, this type of pattern generator must be partitioned. So as compair to LFSR pattern generator the binary counter requires more hardware.

- Modified Counter

Modified counters this method have also been successful as test-pattern generators, but they also require long test sequences.

- *LFSR and ROM*

One of the most important approaches is to use an LFSR as the primary test mode, and then generate test-patterns with an ATPG program for the faults that are missed by the LFSR sequence. These few additional test-patterns can either be stored in a small ROM on the chip for a second test epoch, they can be embedded in the output of the LFSR, or they can be embedded in a scan chain in order to augment the stuck-fault coverage to 100%.

- *Cellular Automaton*

In this method, each pattern generator cell has a few logic gates, a flip-flop, and connections only to

neighboring gates. The cell is replicated to produce the cellular automaton.

Now this paper shows that the most effective methods for Test pattern generator such as LFSR and CA.The Test Pattern Generator components are mostly implemented using either Linear Feed-back Shift Registers (LFSRs) or Cellular Automatons (CA). LFSRs are most commonly used to build TPGs [6] but recently there has been interest in CA for test pattern generation. CA generates test vectors which are more random in nature.

2.1 Linear Feedback Shift Register

LFSR is a linear feedback shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is XOR exclusive-or. Thus by changing the value of seed, the sequence at the output is also change. As register having a finite number of states, it may enter a repeating cycle. Thus LFSR having properly chosen feedback function can produce sequence of random patterns at the output of a repeating cycle. This feedback function is called a
maximum length feedback polynomial.

- LFSR PRNG

Figure 3 shows the basic block diagram of LFSR based on shift register. The feedback from different shift register which influence the input is called taps. This feedback arrangement can be expressed in finite field arithmetic as a polynomial mod 2. The period of sequence is 2n-1, where n is number of shift register.

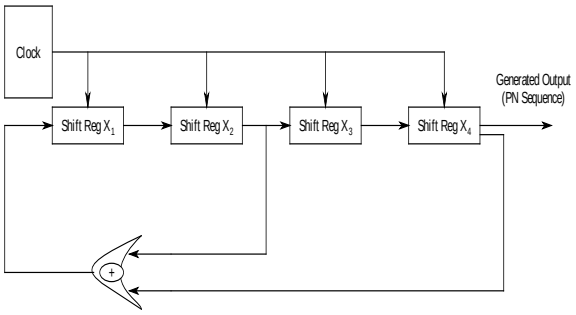
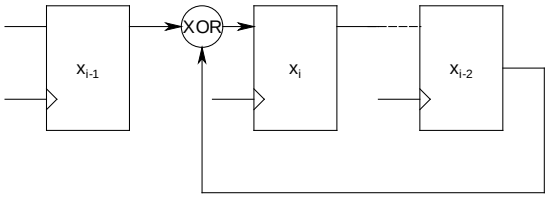


Fig.3. Basic block diagram of LFSR

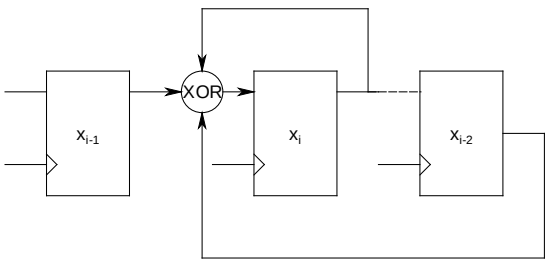
2.2 Cellular Automata

The one of test pattern generator is a Cellular Automata. Cellular automata (CA) are excellent for pattern generation, because they have a better randomness distribution than LFSRs. This method can be invented by John Von Neuman.CA is collection of cell with neighborhood of cell. Every cell in CA simulate is basically built up out of three components. Such as The state, the neighborhood of the cell and the update rule. The state is a current value of the cell which can be Integer or the Boolean. The neighborhood of the cell is the collection of cell to which the cell is connected. These cells can be connected anywhere an grid but the most common type are the ones directly connected to cell itself. The update rule is a function which maps the states of the cell in the neighborhood of cell using a function .Which can be arbitrary complex to a new state of cell. When update rule is the same for cell of grid it is called uniform CA. Apposite non uniform CA where there are different update rule for different location of grid.

It's a collection of cells/nodes formed by flip-flops which are logically related to their nearest neighbors using XOR gates .When the value of a node is deter-mined only by two neighboring cells the CA is known as one-dimensional linear CA (for the rest of the text one-dimensional linear CA is referred as a CA). The logical relations which relate a node to its neighbors are known as rules and they de-fine the characteristics of a CA. There are many rules which can be used to construct a CA register, the most popular being rules 90 and 150 illustrated in figure .[7]



Rule 90
$x_i(t+1)=x_{i-1}(t)$ xor $x_{i+1}(t)$



Rule 150
$x_i(t+1)=x_{i-1}(t)$ xor $x_i(t)$ xor $x_{i+1}(t)$

Fig.4: Cellular Automata Implementation

If cell c only connect with its neighbors , c-1 and c+1, shown in the Figure 2, then the following rule,

called rule 90, can be established based on the following state transition function: Xc(t+1)= Xc-1(t) xor Xc+1(t) and Another relation, rule 150, shown in the Figure 3, is implemented as Xc(t+1) = Xc-1(t) xor Xc(t) xor Xc+1(t).

Figure 5 shows the construction of a 4-bit CA register using rules 90 & 150 and null boundary condition.[7]

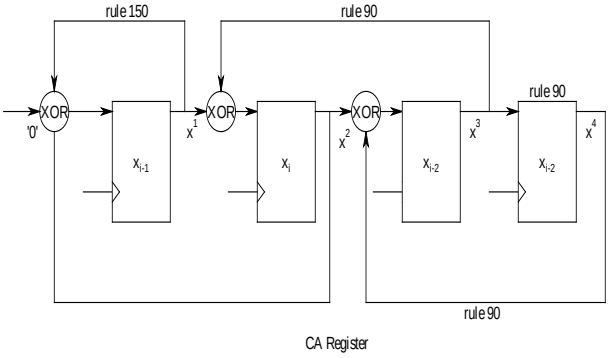


Fig. 5: Cellular Automata Implementation

A CA register is also known as Linear Hybrid Cellular Automata (LHCA) or Linear Cellular Automata Register (LCAR) .Similar to LFSRs there is some combination of rules which produce exhaustive pseudo-random patterns. LHCAs are capable of generating patterns which are more random in nature as compared to an LFSR [3]. But LHCAs have larger nodes and require many more XOR gates as compared to LFSRs. Large number of XOR gates results in higher area over-head of LHCAs. In cases where LHCA is used as a TPG, it is desirable to use a CA for Signature analysis instead of a LFSR.

3. Literature Review

An exhaustive literature review has been carried out related to the work to find out the current research. Abstracts of some of most relevant research works are reported in the following paragraph

A. Shumit saha, Md .Ashikur Rahman, Amit Thakur, "Design and Implementation of a BIST Embedded High speed RS-422 Utilized UART over FPGA," Department of Electronics & Communication Engineering Khulna University of Engineering & Technology, Khulna, Bangladesh July 4-6, 2013, Tiruchengode, India IEEE-31661,

The Author design UART with BIST capability. For Serial data transmission and reception by the UART is used. In order to attain compact, stable and reliable data transmission, the UART is designed. In this paper designed UART, the clock is 20 MHz and time interval for 8 bit data transfer is 2µs. So, time required for per bit transmission is0.25µs which means the baud rate of 4Mbps.The maximum delay is 6.848ns which is much less.RS-422 communication standard is also tested and the bit error rate is only about 0.000007.

B. LixinGao, Yongliang Zhang, Jinhong Zhao "BIST using Cellular Automata as Test Pattern Generator and Response Compaction," School of Information Engineering Guangdong Jidian Polytechnic Guangzhou, China978-1-4577-1415-3/2012 IEEE,

The Author design BIST using Cellular Automata. In this paper author verifies that a CA as a test pattern generator has a maximum length cycle and better properties, and such Ca as a signature analyzer have the same alising properties as linear feedback shift registers.

C. ShumitSaha, Md. Ashikur Rahman, Amit Thakur, " FPGA Implementation of BIST Embedded Inter-Integrated Circuit Bus Protocol".2013International Conference on Electrical and Communication Technology.

The author design and implement the I2C bus Protocol with self-testing ability. In this paper BIST module consist of four blocks. Three are the random pattern generator and a comparator. For random pattern generator author used Linear

Feedback Shift Registers (LFSR).In this paper maximum delay is 5.936ns.

Name	Used Block	Percentage
No. of Slices	41 out of 192	21
No. of Slice Flip flop	44 out of 384	11
No. of 4 input LUT's	72 out of 384	18
No. of IOB's	26 out of 90	28

Table 1: overall analysis

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